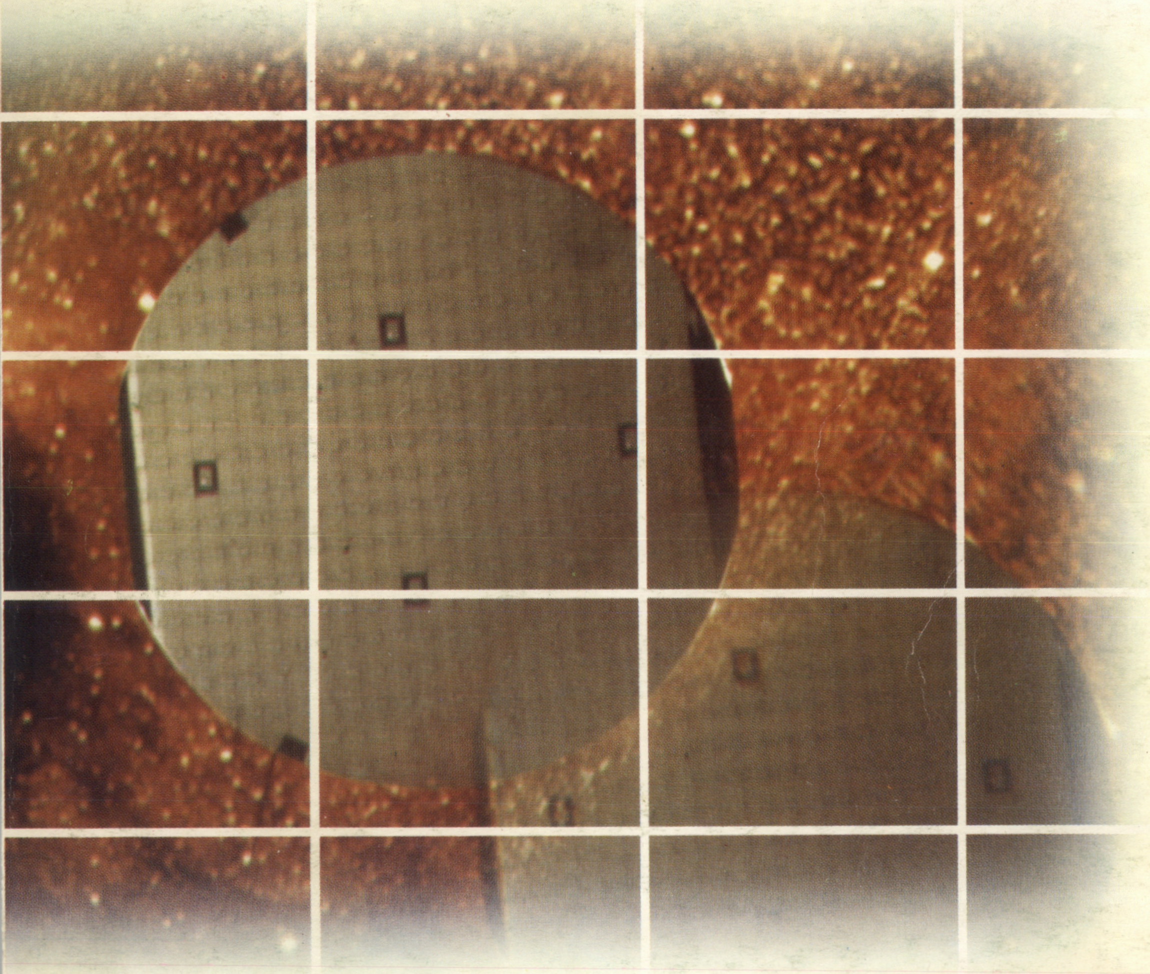
MHS
MATRA-HARRIS SEMICONDUCTEURS



Digital

CMOS HMOS

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Printed in France - Edition 83-11-DI-C-76

Conception et impression Reflets Conseil - Nantes

R.C. 83 B 181 - Tél. (40) 20.10.64

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Devices by Families

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Data Sheet Classifications

CLASSIFICATION	PRODUCT STAGE	DISCLAIMERS
Preview DATA SHEET	Formative or Design	This document contains the design specifications for product under development. Specifications may be changed in any manner without notice.
Advance Information DATA SHEET	Sampling or Pre-Production	This is advanced information, and specifications are subject to change without notice.
Preliminary DATA SHEET	First Production	Supplementary data may be published at a later date. MHS reserves the right to make changes at any time without notice, in order to improve design and supply the best product possible.

I. C. Handling Procedures

I.C. processes produce circuits more rugged than similar ones. However, no semiconductor is immune from damage resulting from the sudden application of many thousands of volts of static electricity. While the phenomenon of catastrophic failure of devices containing MOS transistors or capacitors is well known, even bipolar circuits can be damaged by static discharge, with altered electrical properties and diminished reliability. None of the common I.C internal protection networks operate quickly enough to positively prevent damage.

It is suggested that all semiconductors be handled, tested, and installed using standard "MOS handling techniques" of proper grounding of personnel and equipment. Parts and subassemblies should not be in contact with untreated plastic bags or wrapping material. High impedance I.C. inputs wired to a P.C. connector should have a path to ground on the card.

HANDLING RULES

Since the introduction of integrated circuits with MOS structures and high quality junctions, a safe and effective means of handling these devices has been of primary importance. One method employed to protect gate oxide structures is to incorporate input protection diodes directly on the monolithic chip. However, there is no completely foolproof system of chip input protection in existance in the industry. In addition most compensation networks in linear circuits are located at high impedance nodes, where protection networks would disturb normal circuit operation. If static discharge occurs at sufficient magnitude (2 kV or more), some damage or degradation will usually occur. It has been found that handling equipment and personnel can generate static potentials in excess of 10 KV in a low humidity environment; thus it becomes necessary for additional measures to be implemented to eliminate or reduce static charge. It is evident, therefore, that proper handling procedures or rules should be adopted.

Elimination or reduction of static charge can be accomplished as follows :

- Use conductive work stations. Metallic or conductive plastic* tops on work benches connected to ground help eliminate static build-up.
- Ground all handling equipment.
- Ground all handling personnel with a conductive bracelet through 1-M ohm to ground. The 1-M ohm resistor will prevent electroshock injury to personnel.
- Smocks, clothing, and especially shoes of certain insulating materials (notably nylon) should not be worn in areas where devices are handled. These materials, highly dielectric in nature, will hold, or aid, in the generation of a static change. Where they cannot be eliminated natural materials such as cotton etc. should be used to minimize charge generation capacity.
- Control relative humidity to as high as a level as practical (RH 50 %).
- Ionized air blowers reduce charge build-up in areas where grounding is not possible or desirable.
- Devices should be in conductive carriers during all phases of transport. Leads may be shorted by tubular metallic carriers, conductive foam or foil.
- In automated handling equipment, the belts, chutes, or other surfaces should be of conducting material. If this is not possible, ionized air blowers may be a good alternative.

* Supplier 3M Company "Velostat".

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User's Guide to MOS Static RAMs

SIZE & ORGANIZATION	TYPE	PINS	MHS/ HARRIS	AMD	AMI	EA	FUJITSU	GI	GTE	HITACHI	INMOS	IDT	INTEL	INTERSIL	MICRO POWER SYSTEMS	MITEL	MITSUBISHI	MOSTEK	MOTOROLA	NATIONAL	NEC	OKI	RCA	SIGNETICS	SOLID STATE SCIENTIFIC	SYNERTEK	TI	TOSHIBA	ZILOG
1K	CMOS	18	6561											6561						74C921 6552									
256 × 4	NMOS	16		9112		2112							2112							2112			4112	2112 2606		2112	4043		
		18		2112 9111		2111							2111							2111	2111		4111	2111		2111 2112	4042		
		22		2101 9101		2101		4256					2101							2101	2101		4101	2101		2101	4039		
4K	CMOS	18	6504				8404			4315				6504	6504				6504	6504		5104						5504	
		20																											
4K × 1	NMOS	18		9145 9147	4017 2147		2147		4104 4200	6147 4847			2141 2147	2147				4104 2147	2147	2141 2147	4104 2147			2613		2147	2147 4044 4045	315D	4104 6104
		22		9140				4200																					
4K	CMOS	18	6514				8414			6148 4334				6514	6514	21C14	58981		6514	6514 6848	444	5114 5115	5114					5514	
		20																			445							5047	
1K × 4	NMOS	18		9124 9135 9114	2114				2114 4804	472114 6148			2114 2148	2148				2148	2114 2148	2148 2114	2114	2114		2614		2114	2114 4045 4047	314A	
		20		9148									2142							2141 2142						2142			
		22		9130 9131																									
16K	CMOS	24	6516 65161				MB 8416			6116		IDT 6116							MCM 65116	NMC 6116	µPD 446	MSM 5128	CDM 6116E					5516 5517-18	
2K × 8	NMOS	24					MB 8128						21821				M 58725	4802				2128					4016	2016	
16K × 1	CMOS	24	65261							HM 6167		IDT 6167									µPD 2167								
	NMOS	24					MB 8167				MS 1400		2167					4167	MCM 2167										
4K × 4	CMOS	24	65681							HM 6168		IDT 6168									µPD 2168								
	NMOS	24					MB 8168				MS 1420																		
64K 8K × 8	CMOS	40	6564																										

CMOS Ram Selection guide

BIT \ WORDS	65536	32768	16384	8192	4096	2048	1024	256
8				6564 65641		65161 6116L		
4			6564		65681		6514	6561
1			65261		6504			

CMOS memory 2

Product Index

ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under ''Absolute Maximum Ratings'' may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect devices reliability. The conditions listed under ''Electrical Characteristics'' are the only conditions recommended for satisfactory operation.

Symbols and Abbreviations

This data book utilizes a new set of specification nomenclature. This new format is an IEEE and JEDEC supported standard for semiconductor memories. It is intented to clarify the symbols, abbreviations and definitions, and to make all memory data sheets consistent. We believe that, once acclimated, you will find this standardized format easy to read and use.

ELECTRICAL PARAMETER ABBREVIATIONS

All abbreviations use upper case letters with no subscripts. The initial symbol is one of these four characters :

V (Voltage)
I (Current)
P (Power)
C (Capacitance)

The second letter specifies input (O) or output (O), and the third letter indicates the high (H), low (L) or off (Z) state of the pin during measurements. Examples :

VIL — Input Low Voltage
IOZ — Output Leakage Current

TIMING PARAMETER ABBREVIATIONS

All timing abbreviations use upper case characters with no subscripts. The initial character is always T and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transitions. Thus the format is :

T X X X X

Signal name from which interval is defined
Transition direction for first signal
Signal name to which interval is defined
Transition direction for second signal

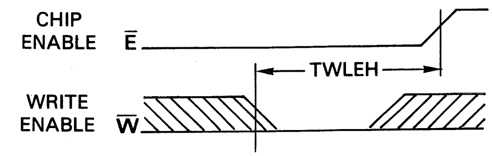
Signal Definitions :

A = Address
D = Data In
Q = Data Out
W = Write Enable
E = Chip Enable
S = Chip Select
G = Output Enable

Transition Définitions :

H = Transition to High
L = Transition to Low
V = Transition to Valid
X = Transition to Invalid or Don't Care
Z = Transition to Off (High Impedance)

EXAMPLE :



The example shows Write pulse setup time defined as TWLEH - Time from Write enable Low to chip Enable High.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address set-up time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS

WAVE-FORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
	—	HIGH IMPEDANCE

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MATRA-HARRIS SEMICONDUCTEURS

data sheet

HM 6116/6116 L
2K × 8
CMOS STATIC RAM

Features

- .ASYNCHRONOUS
- .FAST ACCESS : 120 ns max
- .STAND BY CURRENT : 100 μA max
- .OPERATING SUPPLY CURRENT : 60 mA max
- .DATA RETENTION* : 2 V min *a* 50 μA max
- .STATIC MEMORY CELL
- .INDUSTRY STANDARD PIN OUT
- .HIGH OUTPUT DRIVE : 5 std TTL LS/Load
- .SINGLE SUPPLY : 5 V Vcc
- .TTL COMPATIBLE INPUTS AND OUTPUTS
- .WIDE TEMPERATURE RANGE
- .GATED INPUT BUFFER

Description

.The HM 6116 is a 16384 bits static random access memory organized as 2048 words by 8 bits using CMOS technology and operates from the single 5 V supply.

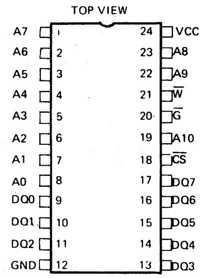
.The HM 6116 use "state of the art" MHS technology : the scaled self aligned junction isolation featuring low stand by current and fast address time.

.The HM 6116 features fully static operation requiring no external clocks or timing strobes, equal access and cycle times.

.8 product available, 100 % screened following MIL STD 883 class B.

* Data retention mode for L version.

Pinout

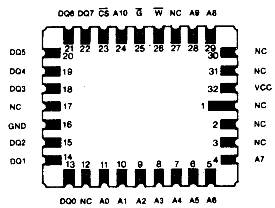


A Address input
DQ Data Input/Output
C̄S̄ Chip Select
Ḡ Output Enable
W Write Enable

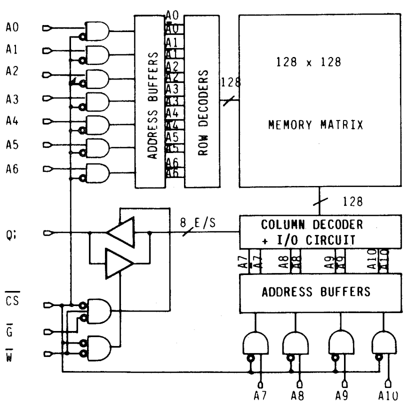
2

LCC

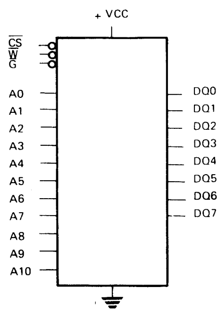
BOTTON VIEW



Functional Diagram



Logic Symbol



• ABSOLUTE MAXIMUM RATINGS

Supply voltage (Vcc-GND) - 0.3V* to + 7V
Input or Output Voltage Applied : (GND-0.3V*) to : (Vcc+0.3V)
Storage temperature : 65° C to + 150° C

* IV pulse width 50 ns

• OPERATING RANGE

	Operating Voltage Range	Operating Temperature
Military (- 2)	4.5V to 5.5V	- 55° to + 125°
Industrial (- 9)	4.5V to 5.5V	- 40 ° to + 85°
Commercial (- 5)	4.5V to 5.5V	0° to 70°

ELECTRICAL CHARACTERISTICS

DC PARAMETERS

SYMBOL	PARAMETER	6116 -5	6116 L-5	6116 -2	6116 L -2	6116 -9	6116 L -9	UNIT	VALUE
ICCSB (1)	standby supply current	3	2	5	4.5	4.5	4.0	mA	max
ICCSB1 (2)	standby supply current	2000	100	3000	1500	1000	500	μA	max
ICCOP (3)	power supply current	70	60	85	80	80	70	mA	max
ICC (4)	average operating supply current	70	60	85	80	80	70	mA	max
II/O (5)	input/output/package current	± 2	± 2	± 10	± 5	± 5	± 2	μA	max
VIL (6)	input low voltage	0.8	0.8	0.8	0.8	0.8	0.8	V	max
VIH (6)	input high voltage	2.2	2.2	VCC-2	VCC-2	2.2	2.2	V	min
VOL (7)	output low voltage	0.4	0.4	0.4	0.4	0.4	0.4	V	max
VOH (7)	output high voltage	2.4	2.4	2.4	2.4	2.4	2.4	V	min
CI (8)	input capitance	8	8	8	8	8	8	PF	max
CO (8)	input/output capitance	10	10	10	10	10	10	PF	max

NOTE 1 : CS = VIH ;Iio = 0 ; input gating
NOTE 2 : $\overline{CS}$ = VCC-0.3V ;Iio = 0
NOTE 3 : ICCOP with a duty cycle = 100 % ; VI = VCC or GND ; IO = 0 ; typical derating = 5 mA/MHz increase in ICCOP
NOTE 4 : $\overline{CS}$ = VIL, II/O = 0 ; addresses and data inputs level = VCC or GND
NOTE 5 : VCC = 5V ; VIN = GND to VCC
NOTE 6 : VIH max = VCC + 0.3V ; VIL min = -IV pulse width 50 ns
NOTE 7 : IOL = 4 mA ; IOH = - 1 mA
NOTE 8 : capacitance sampled and guaranteed not 100 % tested TA = 25° C, f = 1 MHz

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AC PARAMETERS

WRITE CYCLE

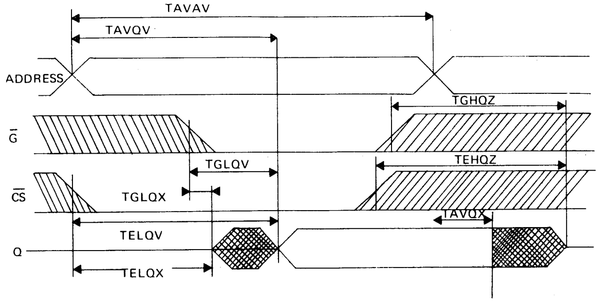
SYMBOL	PARAMETER (1)	6116 -5	6116 L-5	6116 -2	6116 L -2	6116 -9	6116 L -9	UNIT	VALUE
TAVAV	write cycle time	120	120	120	120	120	120	ns	min
TELWH	chip selection to end of write	70	70	70	70	70	70	ns	min
TAVWH	address valid to end of write	105	105	105	105	105	105	ns	min
TAVWL	address setup time	20	20	20	20	20	20	ns	min
TWLWH	write pulse width	70	70	70	70	70	70	ns	min
TWHAV	write recovery time	5	5	5	5	5	5	ns	max
TGHOZ	output enable to output in high Z	40	40	40	40	40	40	ns	max
TWLOZ	write low to output in high Z	50	50	50	50	50	50	ns	min
TDVWH	input data valid to write high	35	35	35	35	35	35	ns	min
TWHDX	data hold from write time	5	5	5	5	5	5	ns	min
TWHQX	output active from end of write	5	5	5	5	5	5	ns	min
TWLEH	write low to chip select high	70	70	70	70	70	70	ns	min
TDVEH	input data valid to chip select high	35	35	35	35	35	35	ns	min

READ CYCLE

SYMBOL	PARAMETER (1)	6116 -5	6116 L-5	6116 -2	6116 L -2	6116 -9	6116 L -9	UNIT	VALUE
TAVAV	read cycle time	120	120	120	120	120	120	ns	min
TAVQV	address access time	120	120	120	120	120	120	ns	max
TELQV	chip select access time	120	120	120	120	120	120	ns	max
TELQX	chip select low to active output	10	10	10	10	10	10	ns	min
TGLQV	output enable to output valid time	80	80	80	80	80	80	ns	max
TGLQX	output enable to output in low Z time	10	10	10	10	10	10	ns	min
TEHQZ	chip select disable time	40	40	40	40	40	40	ns	max
TGHOZ	output enable to output in high Z time	40	40	40	40	40	40	ns	max
TAVQX	output holdtime from address change	10	10	10	10	10	10	ns	min

NOTE 1 : LOAD : 100 pf (including JIG) AND TTL GATE

1. READ CYCLE

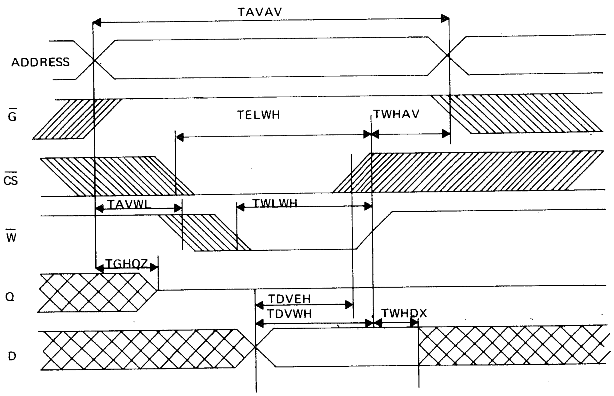


TRUTH TABLE :

$\overline{CS}$	$\overline{G}$	$\overline{W}$	D	Q	POWER SUPPLY CURRENT	MODE
H	X	X	Z	Z	ICCSB	$\overline{CS}$=VIH DESELECT
H	X	X	Z	Z	ICCSB1	$\overline{CS}$>Vcc-0.3 DESELECT
L	L	H	Z	VALID	ICC	READ
L	H	L	VALID	Z	ICC	WRITE
L	L	L	VALID	Z	ICC	WRITE
L	H	H	Z	Z	ICC	DESELECT

NOTE : $\overline{W}$ IS HIGH FOR A READ CYCLE

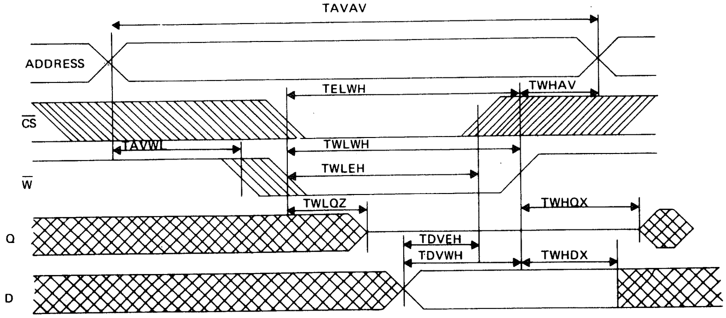
3. WRITE CYCLE TIME 1



This write cycle time is recommended for continuous writing.

$\overline{G}$ = VIH during this write cycle.

3. WRITE CYCLE TIME 2



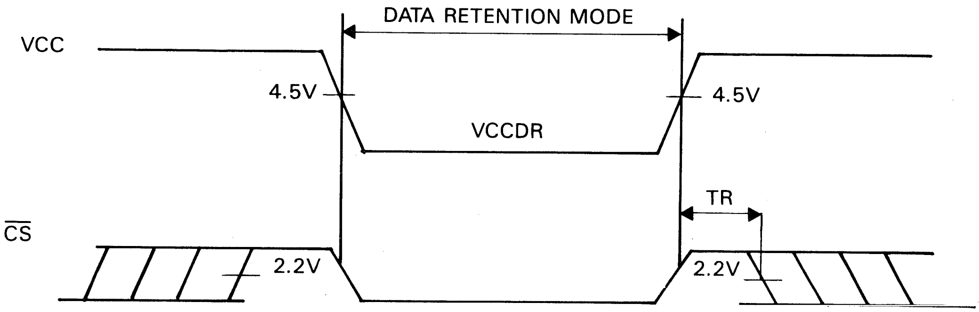
NOTE : $\overline{G}$ IS LOW THROUGHOUT WRITE CYCLE.

This write cycle time may be used for write and read in the same cycle (write followed by read).

Data retention Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	6116L -5		6116L -9		6116L -2		UNIT
			min	max	min	max	min	max	
VCC for data retention	VCCDR	CS=VCC VIN=OV or VCC	2	–	2	–	2	–	V
data retention current	ICCDR	VCC=2.0V, CS=VCC VIN=OV or VCC	–	50	–	200	–	600	μA
operating recovery time	TR		TAVAV		TAVAV		TAVAV		

TAVAV = read cycle time



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Ordering Information

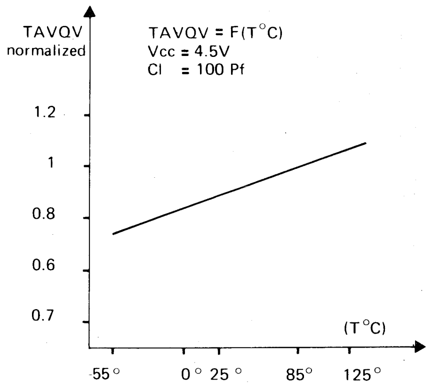
DEVICE TYPE	PACKAGE	TEMPERATURE RANGE
HM1 - 6116 (L) -5	CERAMIC DIL	0° C to + 70° C
HM1 - 6116 (L) -9	CERAMIC DIL	–40° C to + 85° C
HM1 - 6116 (L) -2	CERAMIC DIL	–55° C to +125° C
HM1 - 6116 (L) -8	CERAMIC DIL	–55° C to +125° C
HM3 - 6116 (L) -5	PLASTIC DIL	0° C to + 70° C
HM3 - 6116 (L) -9	PLASTIC DIL	–40° C to + 85° C
HM4 - 6116 (L) -5	LCC 32 PINS	0° C to + 70° C
HM4 - 6116 (L) -9	LCC 32 PINS	–40° C to + 85° C
HM4 - 6116 (L) -2	LCC 32 PINS	–55° C to +125° C
HM4 - 6116 (L) -8	LCC 32 PINS	–55° C to +125° C

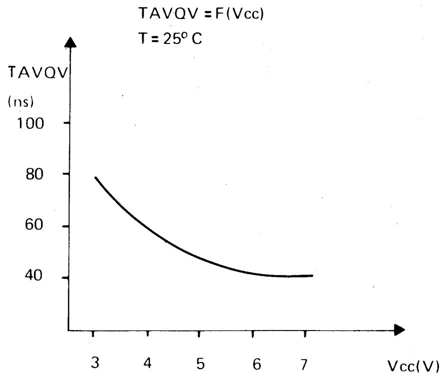
TEMPERATURE RANGE (-5, -9, -2, -8)

Blank : Standard
L Low power part] DEVICE TYPE

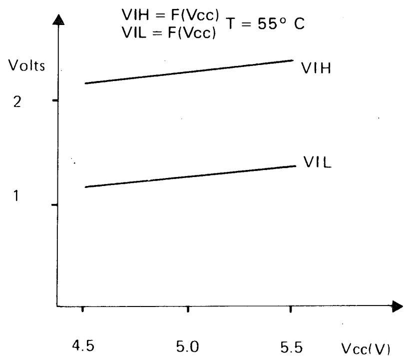
PACKAGE (1, 3, 4)

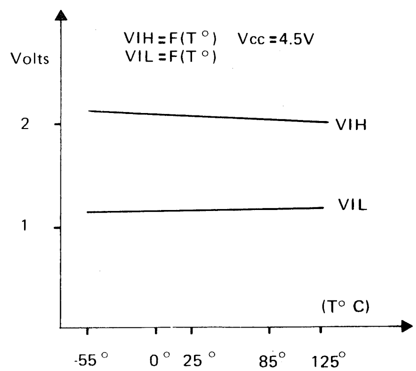
READ CYCLE TIME



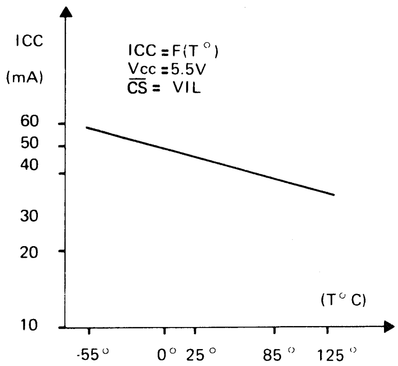


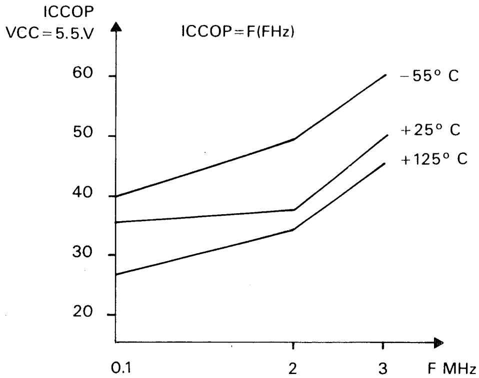
INPUT VOLTAGE





POWER SUPPLY CURRENT





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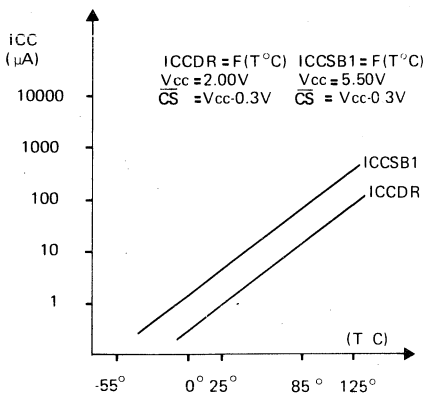
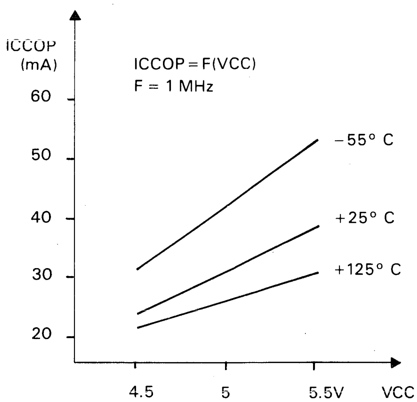
STANDBY AND DATA RETENTION CURRENT





MHS MATRA-HARRIS SEMICONDUCTEURS

data sheet

HM-6504
4096 × 1 CMOS RAM

Features

- LOW POWER STANDBY 250µW MAX.
- LOW POWER OPERATION 35mW/MHz MAX.
- EXTREMELY LOW SPEED POWER PRODUCT
- DATA RETENTION @ 2.0V MIN.
- TTL COMPATIBLE INPUT/OUTPUT
- THREE-STATE OUTPUT
- STANDARD JEDEC PINOUT
- FAST ACCESS TIME 200nsec MAX.
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON CHIP ADDRESS REGISTER

Description

The HM-6504 is a 4096 x 1 static CMOS RAM fabricated using self aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

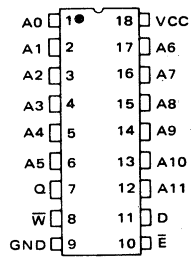
On chip latches are provided for addresses, data input and data output allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance for use in expanded memory arrays.

The HM-6504 is a fully static RAM and may be maintained in any state for an indefinite period of time.

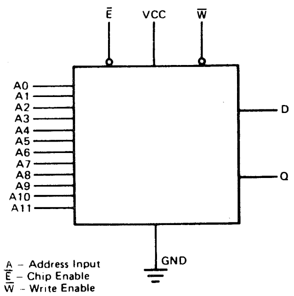
Data retention supply voltage and supply current are guaranteed over temperature.

Pinout

TOP VIEW

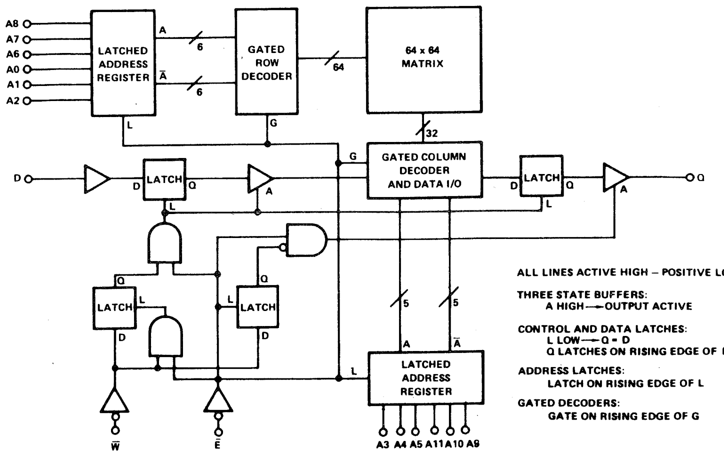


Logic Symbol



A – Address Input
Ē – Chip Enable
W̄ – Write Enable
D – Data Input
Q – Data Output

Functional Diagram



ALL LINES ACTIVE HIGH – POSITIVE LOGIC

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

CONTROL AND DATA LATCHES:
L LOW → Q = D
Q LATCHES ON RISING EDGE OF L

ADDRESS LATCHES:
LATCH ON RISING EDGE OF L

GATED DECODERS:
GATE ON RISING EDGE OF G

CAUTION : These devices are sensitive to electro-static discharge.

Symbols and Abbreviations

This data sheet utilizes a new set of specification nomenclature. This new format is an IEEE and JEDEC supported standard for semiconductor memories. It is intended to clarify the symbols, abbreviations and definitions, and to make all memory data sheets consistent. We believe that, once acclimated, you will find this standardized format easy to read and use.

ELECTRICAL PARAMETER ABBREVIATIONS

All abbreviations use upper case letters with no subscripts. The initial symbol is one of these four characters:

- V (Voltage)
- I (Current)
- P (Power)
- C (Capacitance)

The second letter specifies input (I) or output (O), and the third letter indicates the high (H), low (L) or off (Z) state of the pin during measurements. Examples:

VIL — Input Low Voltage
IOZ — Output Leakage Current

TIMING PARAMETER ABBREVIATIONS

All timing abbreviations use upper case characters with no subscripts. The initial character is always T and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transitions. Thus the format is:

T X X X X

- Signal name from which interval is defined
- Transition direction for first signal
- Signal name to which interval is defined
- Transition direction for second signal

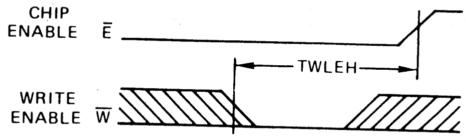
Signal Definitions:

- A = Address
- D = Data In
- Q = Data Out
- W = Write Enable
- E = Chip Enable
- S = Chip Select
- G = Output Enable

Transition Definitions:

- H = Transition to High
- L = Transition to Low
- V = Transition to Valid
- X = Transition to Invalid or Don't Care
- Z = Transition to Off (High Impedance)

EXAMPLE:

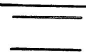
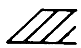
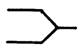


The example shows Write pulse setup time defined as TWLEH-Time from Write enable Low to chip Enable High.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address set-up time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	—	HIGH IMPEDANCE

ABSOLUTE MAXIMUM RATINGS

Supply Voltage - (VCC - GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	TEMP = 25°C (1) VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50	1.0	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current (2)		7	5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		25	0.1	μA	VCC = 2.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.45	0.35	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance (3)		10.0	6.0	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		200	150	ns	(4)
	TAVQV	Address Access Time		220	150	ns	(4)
	TELQX	Chip Enable Output Enable Time		80	40	ns	(4)
	TWLQZ	Write Enable Output Disable Time	20	80	40	ns	(4)
	TEHQZ	Chip Enable Output Disable Time		80	40	ns	(4)
	TELEH	Chip Enable Pulse Negative Width	200		150	ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	90		60	ns	(4)
	TAVEL	Address Setup Time	20		0	ns	(4)
	TELAX	Address Hold Time	50		20	ns	(4)
	TWLWH	Write Enable Pulse Width	200		100	ns	(4)
	TWLEH	Write Enable Pulse Setup Time	200		100	ns	(4)
	TELWH	Write Enable Pulse Hold Time	200		150	ns	(4)
	TDVWH	Data Setup Time	120		80	ns	(4)
	TWHDZ	Data Hold Time	0		0	ns	(4)
	TWLDV	Write Data Delay Time	80		50	ns	(4)
	TWLEL	Early Output High-Z Time	0		-10	ns	(4)
	TEHWH	Late Output High-Z Time	0		-10	ns	(4)
	TELEL	Read or Write Cycle Time	290		210	ns	(4)

NOTES:
1. All devices tested at worst case limits. Room Temp., 5V data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Ex: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC test conditions: Inputs – TRISE = TFALL = 20ns; Output – CLOAD = 50pF. All timing measured at 1.5V reference level.

2

ABSOLUTE MAXIMUM RATINGS

Supply Voltage – (VCC -GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	TEMP = 25°C (1) VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50	1.0	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current (2)		7	5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		25	0.1	μA	IO = 0, VCC = 2.0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance (3)		10.0	6.0	pF	f = 1MHz VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		300	170	ns	(4)
	TAVQV	Address Access Time		320	170	ns	(4)
	TELQX	Chip Enable Output Enable Time	20	100	40	ns	(4)
	TEHQZ	Chip Enable Output Disable Time		100	40	ns	(4)
	TELEH	Chip Enable Pulse Negative Width	300		170	ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	120		70	ns	(4)
	TAVEL	Address Setup Time	20		0	ns	(4)
	TELAX	Address Hold Time	50		20	ns	(4)
	TWLWH	Write Enable Pulse Width	80		40	ns	(4)
	TWLEH	Write Enable Pulse Setup Time	200		130	ns	(4)
	TWLEL	Early Write Pulse Setup Time	0		-10	ns	(4)
	TWHEL	Write Enable Read Mode Setup Time	0		-10	ns	(4)
	TELWH	Early Write Pulse Hold Time	80		40	ns	(4)
	TDVWL	Data Setup Time	0		0	ns	(4)
	TDVEL	Early Write Data Setup Time	0		0	ns	(4)
	TWLDX	Data Hold Time	80		40	ns	(4)
	TELDX	Early Write Data Hold Time	80		40	ns	(4)
	TQVWL	Data Valid to Write Time	0		0	ns	(4)
	TELEL	Read or Write Cycle Time	420		240	ns	(4)

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC Test Conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage – (VCC -GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage Industrial (-9)	4.5V to 5.5V
Operating Temperature Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP = 25°C (1) VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100	10	µA	IO = 0, VI = VCC or GND
	ICCOP	Operating Supply Current (2)		7	5	mA	f = 1MHz, IO = 0, VI = VCC or GND
	ICCDR	Data Retention Supply Current		50	25	µA	IO = 0 VCC = 2.0V, VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0	pF	f = 1MHz, VI = VCC or GND
	CO	Output Capacitance (3)		10.0	6.0	pF	f = 1MHz, VO= VCC or GND
A.C.	TELQV	Chip Enable Access Time		300	170	ns	(4)
	TAVQV	Address Access Time		320	170	ns	(4)
	TELQX	Chip Enable Output Enable Time	20	100	40	ns	(4)
	TEHQZ	Chip Enable Output Disable Time		100	40	ns	(4)
	TELEH	Chip Enable Pulse Negative Width	300		170	ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	120		70	ns	(4)
	TAVEL	Address Setup Time	20		0	ns	(4)
	TELAX	Address Hold Time	50		20	ns	(4)
	TWLWH	Write Enable Pulse Width	80		40	ns	(4)
	TWLEH	Write Enable Pulse Setup Time	200		130	ns	(4)
	TWLEL	Early Write Pulse Setup Time	0		-10	ns	(4)
	TWHEL	Write Enable Read Mode Setup Time	0		-10	ns	(4)
	TELWH	Early Write Pulse Hold Time	80		40	ns	(4)
	TDVWL	Data Setup Time	0		0	ns	(4)
	TDVEL	Early Write Data Setup Time	0		0	ns	(4)
	TWLDX	Data Hold Time	80		40	ns	(4)
	TELDX	Early Write Data Hold Time	80		40	ns	(4)
	TQVWL	Data Valid to Write Time	0		0	ns	(4)
	TELEL	Read or Write Cycle Time	420		240	ns	(4)

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC Test Conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage – (VCC - GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (GND +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

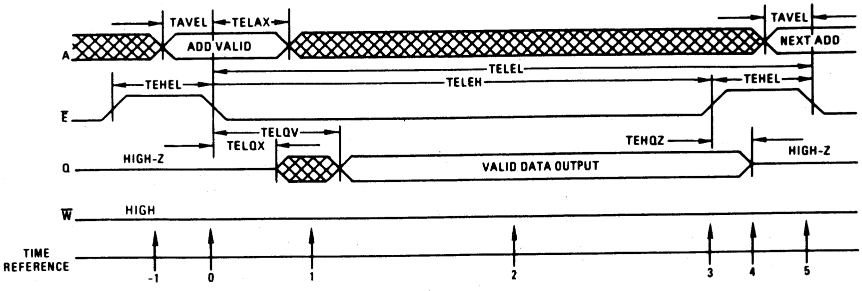
Operating Supply Voltage Commercial	4.5V to 5.5V
Operating Temperature Commercial	0°C to +75°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	TEMP = 25°C ① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		500	50	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		7	5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		500	10	μA	VCC = 2.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-10.0	+10.0	±0.5	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-10.0	+10.0	±0.5	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -0.4mA
	CI	Input Capacitance ③		8.0	5.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance ③		10.0	6.0	pF	f = 1MHz VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		350	200	ns	④
	TAVQV	Address Access Time		370	200	ns	④
	TELQX	Chip Enable Output Enable Time	20	100	50	ns	④
	TEHQZ	Chip Enable Output Disable Time		100	50	ns	④
	TELEH	Chip Enable Pulse Negative Width	350		200	ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		100	ns	④
	TAVEL	Address Setup Time	20		0	ns	④
	TELAX	Address Hold Time	50		20	ns	④
	TWLWH	Write Enable Pulse Width	100		60	ns	④
	TWLEH	Write Enable Pulse Setup Time	250		100	ns	④
	TWLEL	Early Write Pulse Setup Time	0		-10	ns	④
	TWHEL	Write Enable Read Setup Time	0		-10	ns	④
	TELWH	Early Write Pulse Hold Time	100		60	ns	④
	TDVWL	Data Setup Time	30		0	ns	④
	TDVEL	Early Write Data Setup Time	30		0	ns	④
	TWLDX	Data Hold Time	100		60	ns	④
	TELDX	Early Write Data Hold Time	100		80	ns	④
	TQVWL	Data Valid to Write Time	0		0	ns	④
	TELEL	Read or Write Cycle Time	500		300	ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC Test Conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.

Read Cycle

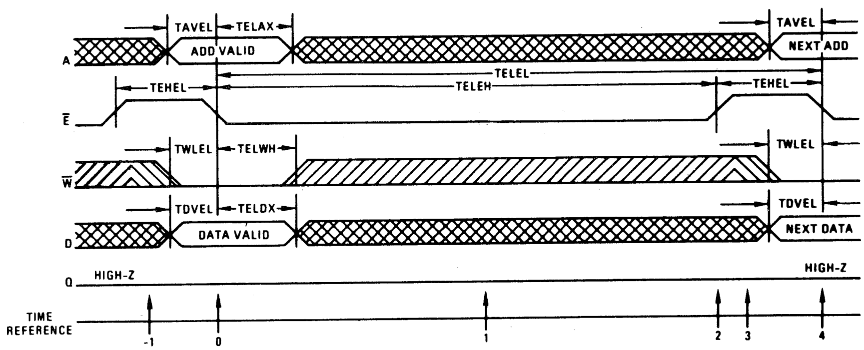


TRUTH TABLE

TIME REFERENCE	INPUTS E	INPUTS W	INPUTS A	OUTPUT Q	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	OUTPUT ENABLED
2	L	H	X	V	OUTPUT VALID
3	↗	H	X	V	READ ACCOMPLISHED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until during time (T = 2). $\overline{W}$ must remain high until after time (T = 2). After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the output buffer and ready the RAM for the next memory cycle (T = 4).

Early Write Cycle

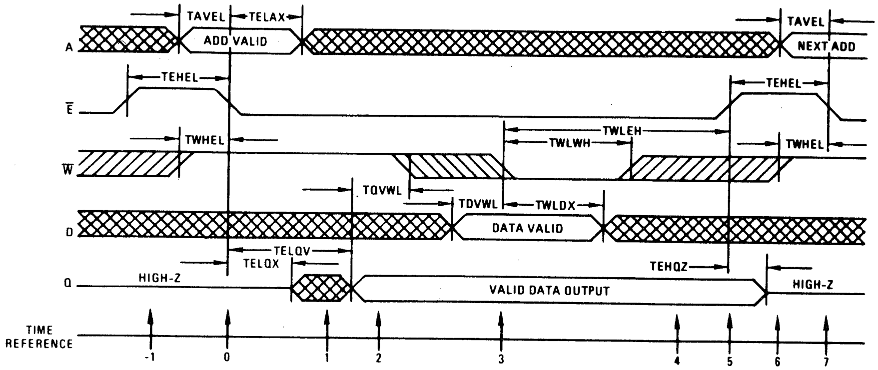


TRUTH TABLE

TIME REFERENCE	INPUTS E	INPUTS W	INPUTS A	INPUTS D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	L	V	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	X	X	X	Z	WRITE IN PROGRESS INTERNALLY
2	↗	X	X	X	Z	WRITE COMPLETED
3	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
4	↘	L	V	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The early write cycle is the only cycle where the output is guaranteed not to become active. On the falling edge of $\overline{E}$ (T = 0), the addresses, the write signal, and the data input are latched in on chip registers. The logic value of $\overline{W}$ at the time $\overline{E}$ falls determines the state of the output buffer for that cycle. Since $\overline{W}$ is low when $\overline{E}$ falls, the output buffer is latched into the high impedance state and will remain in that state until $\overline{E}$ returns high (T = 2). For this cycle, the data input is latched by $\overline{E}$ going low; therefore data set up and hold times should be referenced to $\overline{E}$. When $\overline{E}$ (T = 2) returns to the high state the output buffer disables and all signals are unlatched. The device is now ready for the next cycle.

Read Modify Write Cycle



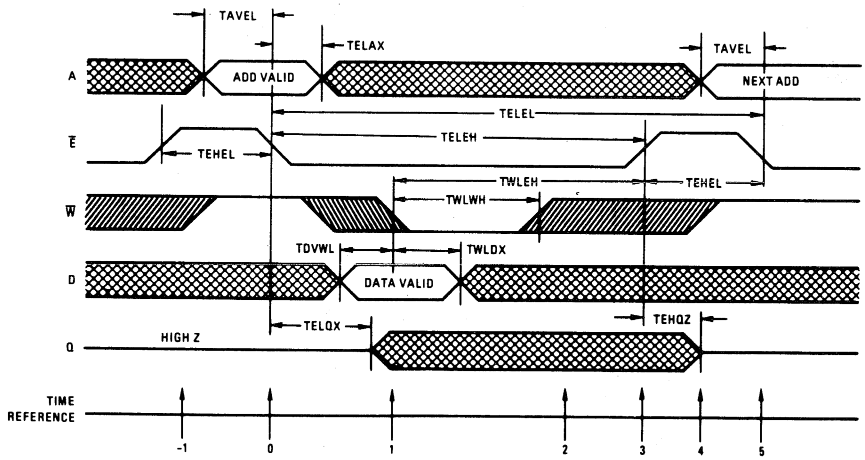
TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	⤵	H	V	X	Z	CYCLE BEGINS, ADDRESS ARE LATCHED
1	L	H	X	X	X	OUTPUT ENABLED
2	L	H	X	X	V	OUTPUT VALID, READ AND MODIFY TIME
3	L	⤵	X	V	V	WRITE BEGINS, DATA IS LATCHED
4	L	X	X	X	V	WRITE IN PROGRESS INTERNALLY
5	⤴	X	X	X	V	WRITE COMPLETED
6	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
7	⤵	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

2

The read modify write cycle begins as all other cycles on the falling edge of $\overline{E}$ (T= 0). The $\overline{W}$ line should be high at (T = 0) in order to latch the output buffers in the active state. During (T = 1) the output will be active but not valid until (T = 2). On the falling edge of the $\overline{W}$ (T = 3) the data present at the output and input are latched. The $\overline{W}$ signal also latches itself on its low going edge. All input signals excluding $\overline{E}$ have been latched and have no further effect on the RAM. The rising edge of $\overline{E}$ (T = 5) completes the write portion of the cycle and unlatches all inputs and output . The output goes to a high impedance and the RAM is ready for the next cycle.

Late Write Cycle



TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	H	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	↘	X	V	X	WRITE BEGINS, DATA IS LATCHED
2	L	H	X	X	X	WRITE IN PROGRESS INTERNALLY
3	↗	H	X	X	X	WRITE COMPLETED
4	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The late write cycle is a cross between the early write cycle and the read-modify-write cycle.

Recall that in the early write the output is guaranteed to remain high impedance, and in the read-modify-write the output is guaranteed valid at access time. The late write is between these two cases. With this cycle the output may become active, and may become valid data, or may remain active but undefined. Valid data is written into the RAM if data set up, data hold, write setup and write pulse widths are observed.

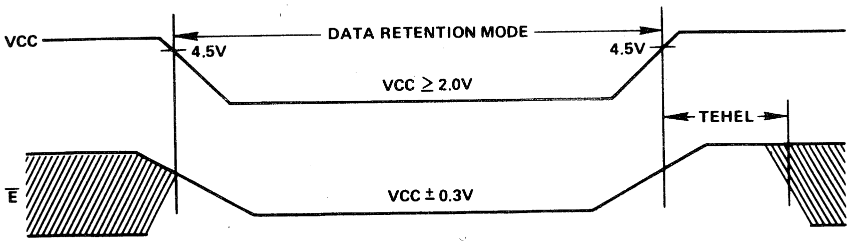
NOTES:
In the above descriptions the numbers in parenthesis (T = n) refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

Low Voltage Data Retention

MHS CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC + 0.3V to VCC - 0.3V.
2. On RAMs which have selects or output enables (e.g. $\overline{S}$, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. All other inputs should be held either high (at CMOS VCC) or at ground to minimize ICCDR.
4. Inputs which are to be held high (e.g. $\overline{E}$) must be kept between VCC + 0.3V and 70% of VCC during the power up and power down transitions.
5. The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 volts).

DATA RETENTION TIMING



Ordering Information

Example: HM 1 – 6504 – 9

- HM — MHS MEMORY
- 1 — PACKAGE
- 6504 — DEVICE
- 9 — VERSION/TEMP. RANGE

		TEMPERATURE RANGE		
		MILITARY	INDUSTRIAL	COMMERCIAL
PACKAGE		- 2	- 9	- 5
CERDIP	1 -	YES	YES	YES
EPOXY	3 -	NO	YES	YES
LEADLESS	4-	YES	YES	YES

MHS MATRA-HARRIS SEMICONDUCTEURS

data sheet

HM-6514
1024 × 4 CMOS RAM

Features

- LOW POWER STANDBY — 250μW MAX.
- LOW POWER OPERATION — 35mW/MHz MAX.
- DATA RETENTION — @ 2.0V MIN.
- TTL COMPATIBLE INPUT/OUTPUT
- COMMON DATA IN/OUT
- THREE-STATE OUTPUTS
- STANDARD JEDEC PINOUT
- FAST ACCESS TIME — 200nsec MAX.
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON CHIP ADDRESS REGISTER

Description

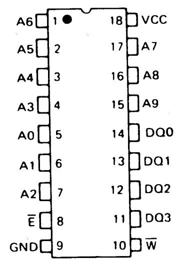
The HM-6514 is a 1024 x 4 static CMOS RAM fabricated using self aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

On chip latches are provided for the addresses allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory systems.

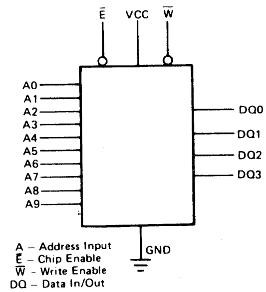
The HM-6514 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

Pinout

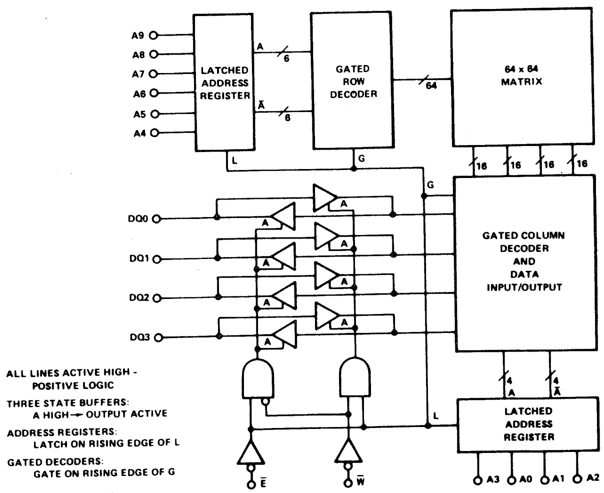
TOP VIEW



Logic Symbol



Functional Diagram



CAUTION: These devices are sensitive to electro-static discharge.

Symbols and Abbreviations

This data sheet utilizes a new set of specification nomenclature. This new format is an IEEE and JEDEC supported standard for semiconductor memories. It is intended to clarify the symbols, abbreviations and definitions, and to make all memory data sheets consistent. We believe that, once acclimated, you will find this standardized format easy to read and use.

ELECTRICAL PARAMETER ABBREVIATIONS

All abbreviations use upper case letters with no subscripts. The initial symbol is one of these four characters:

V (Voltage)
I (Current)
P (Power)
C (Capacitance)

The second letter specifies input (I) or output (O), and the third letter indicates the high (H), low (L) or off (Z) state of the pin during measurements. Examples:

VIL — Input Low Voltage
IOZ — Output Leakage Current

TIMING PARAMETER ABBREVIATIONS

All timing abbreviations use upper case characters with no subscripts. The initial character is always T and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transitions. Thus the format is:

T X X X X

Signal name from which interval is defined
Transition direction for first signal
Signal name to which interval is defined
Transition direction for second signal

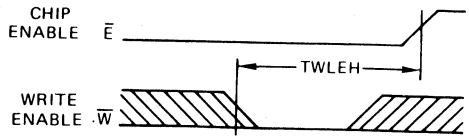
Signal Definitions:

A = Address
D = Data In
Q = Data Out
W = Write Enable
E = Chip Enable
S = Chip Select
G = Output Enable

Transition Definitions:

H = Transition to High
L = Transition to Low
V = Transition to Valid
X = Transition to Invalid or Don't Care
Z = Transition to Off (High Impedance)

EXAMPLE:

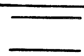
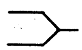


The example shows Write pulse setup time defined as TWLEH-Time from Write enable Low to chip Enable High.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address set-up time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	—	HIGH IMPEDANCE

ABSOLUTE MAXIMUM RATINGS

Supply Voltage - (VCC - GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP = 25°C (1) VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50	1.0	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current (2)		7	5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		25	0.1	μA	IO = 0 VCC = 2.0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance (3)		10.0	6.0	pF	f = 1MHz VO= VCC or GND
A.C.	TELQV	Chip Enable Access Time		200	150	ns	(4)
	TAVQV	Address Access Time		220	150	ns	(4)
	TELQX	Chip Enable Output Enable Time	20	80	40	ns	(4)
	TEHQZ	Chip Enable Output Disable Time		80	40	ns	(4)
	TELEH	Chip Enable Pulse Negative Width	200		150	ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	90		60	ns	(4)
	TAVEL	Address Setup Time	20		0	ns	(4)
	TELAX	Address Hold Time	50		20	ns	(4)
	TWLWH	Write Enable Pulse Width	60		40	ns	(4)
	TWLEH	Write Enable Pulse Setup Time	150		100	ns	(4)
	TWLEL	Early Write Pulse Setup Time	0		-10	ns	(4)
	TWHEL	Write Enable Read Mode Setup Time	0		-10	ns	(4)
	TELWH	Early Write Pulse Hold Time	60		40	ns	(4)
	TDVWL	Data Setup Time	0		0	ns	(4)
	TDVEL	Early Write Data Setup Time	0		0	ns	(4)
	TWLDX	Data Hold Time	60		40	ns	(4)
	TELDX	Early Write Data Hold Time	60		40	ns	(4)
	TQVWL	Data Valid to Write Time	0		0	ns	(4)
	TELEL	Read or Write Cycle Time	290		210	ns	(4)

NOTES:
1. All devices tested at worst case limits. Room Temp., 5V data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Ex: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC test conditions: Inputs — TRISE = TFALL = 20ns; Output — CLOAD = 50pF. All timing measured at 1.5V reference level.

2

ABSOLUTE MAXIMUM RATINGS

Supply Voltage – (VCC -GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (GND +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	TEMP = 25°C (1) VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50	1.0	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current (2)		7	5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		25	0.1	μA	VCC = 2.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.45	0.35	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance (3)		10.0	6.0	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300	170	ns	(4)
	TAVQV	Address Access Time		320	170	ns	(4)
	TELQX	Chip Enable Output Enable Time		100	40	ns	(4)
	TWLQZ	Write Enable Output Disable Time	20	100	40	ns	(4)
	TEHQZ	Chip Enable Output Disable Time		100	40	ns	(4)
	TELEH	Chip Enable Pulse Negative Width	300		170	ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	120		70	ns	(4)
	TAVEL	Address Setup Time	20		0	ns	(4)
	TELAX	Address Hold Time	50		20	ns	(4)
	TWLWH	Write Enable Pulse Width	300		150	ns	(4)
	TWLEH	Write Enable Pulse Setup Time	300		150	ns	(4)
	TELWH	Write Enable Pulse Hold Time	300		150	ns	(4)
	TDVWH	Data Setup Time	200		100	ns	(4)
	TWHDZ	Data Hold Time	0		0	ns	(4)
	TWLDV	Write Data Delay Time	100		50	ns	(4)
	TWLEL	Early Output High-Z Time	0		-10	ns	(4)
	TEHWH	Late Output High-Z Time	0		-10	ns	(4)
	TELEL	Read or Write Cycle Time	420		240	ns	(4)

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC Test Conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage – (VCC -GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (GND +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage Industrial (-9)	4.5V to 5.5V
Operating Temperature Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP = 25°C (1) VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100	10	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current (2)		7	5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		50	0.1	μA	VCC = 2.0V, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.45	0.35	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance (3)		10.0	6.0	pF	VIO= VCC or GND f = 1MHz.
A.C.	TELQV	Chip Enable Access Time		300	170	ns	(4)
	TAVQV	Address Access Time		320	170	ns	(4)
	TELQX	Chip Enable Output Enable Time		100	40	ns	(4)
	TWLQZ	Write Enable Output Disable Time	20	100	40	ns	(4)
	TEHQZ	Chip Enable Output Disable Time		100	40	ns	(4)
	TELEH	Chip Enable Pulse Negative Width	300		170	ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	120		70	ns	(4)
	TAVEL	Address Setup Time	20		0	ns	(4)
	TELAX	Address Hold Time	50		20	ns	(4)
	TWLWH	Write Enable Pulse Width	300		150	ns	(4)
	TWLEH	Write Enable Pulse Setup Time	300		150	ns	(4)
	TELWH	Write Enable Pulse Hold Time	300		170	ns	(4)
	TDVWH	Data Setup Time	200		100	ns	(4)
	TWHDZ	Data Hold Time	0		0	ns	(4)
	TWLDV	Write Data Delay Time	100		50	ns	(4)
	TWLEL	Early Output High-Z Time	0		-10	ns	(4)
	TEHWH	Late Output High-Z Time	0		-10	ns	(4)
	TELEL	Read or Write Cycle Time	420		240	ns	(4)

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC Test Conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.

ABSOLUTE MAXIMUM RATINGS	
Supply Voltage – (VCC - GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (GND +0.3V)
Storage Temperature	-65°C to +150°C

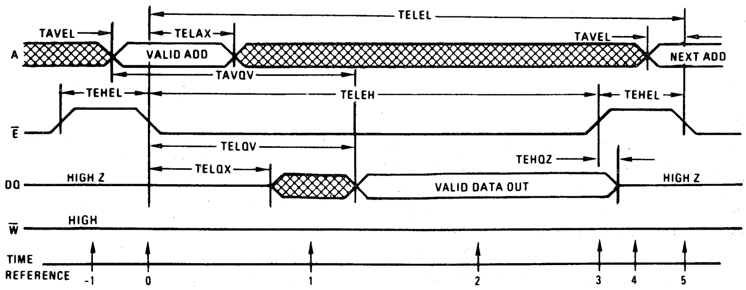
OPERATING RANGE	
Operating Supply Voltage Commercial	4.5V to 5.5V
Operating Temperature Commercial	0°C to +75°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP = 25°C (1) VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		500	50	μA	VI = VCC or GND IO = 0
	ICCOP	Operating Supply Current (2)		7	5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		500	10	μA	VCC = 2.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-10.0	+10.0	±0.5	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-10.0	+10.0	±0.5	μA	VCC ≤ VIO ≤ GND
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.45	0.35	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -0.4mA
	CI	Input Capacitance (3)		8.0	5.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance (3)		10.0	6.0	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		350	200	ns	(4)
	TAVQV	Address Access Time		370	200	ns	(4)
	TELQX	Chip Enable Output Enable Time	20	100	50	ns	(4)
	TWLQZ	Write Enable Output Disable Time		100	50	ns	(4)
	TEHQZ	Chip Enable Output Disable Time		100	50	ns	(4)
	TELEH	Chip Enable Pulse Negative Width	350		200	ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	150		100	ns	(4)
	TAVEL	Address Setup Time	20		0	ns	(4)
	TELAX	Address Hold Time	50		20	ns	(4)
	TWLWH	Write Enable Pulse Width	350		200	ns	(4)
	TWLEH	Write Enable Pulse Setup Time	350		200	ns	(4)
	TELWH	Write Enable Pulse Hold Time	350		200	ns	(4)
	TDVWH	Data Setup Time	250		150	ns	(4)
	TWHDZ	Data Hold Time	0		0	ns	(4)
	TWLDV	Write Data Delay Time	100		50	ns	(4)
	TWLEL	Early Output High-Z Time	0		-10	ns	(4)
	TEHWH	Late Output High-Z Time	0		-10	ns	(4)
	TELEL	Read or Write Cycle Time	500		320	ns	(4)

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC Test Conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.

Read Cycle



TRUTH TABLE

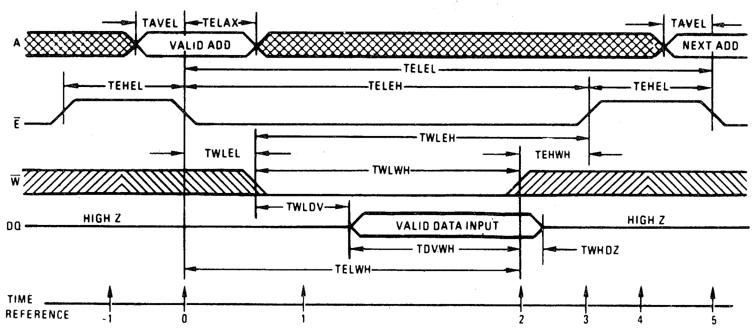
TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	DATA I/O DQ	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	⌄	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	OUTPUT ENABLED
2	L	H	X	V	OUTPUT VALID
3	⌃	H	X	V	READ ACCOMPLISHED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	⌄	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time the addresses may change state without affecting device operation. During time (T = 1) the outputs become enabled but data is not valid until time (T = 2).

$\overline{W}$ must remain high throughout the read cycle. After the data has been read $\overline{E}$ may return high (T = 3). This will force the output buffers into a high impedance mode at time (T = 4). The memory is now ready for the next cycle.

2

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	DQ	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	⌄	X	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	X	Z	WRITE PERIOD BEGINS
2	L	⌃	X	V	DATA IN IS WRITTEN
3	⌃	H	X	Z	WRITE COMPLETED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	⌄	X	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The write cycle is initiated by the falling edge of $\overline{E}$ (T = 0), which latches the address information in the on chip registers. There are two basic types of write cycles, which differ in the control of the common data-in/data-out bus.

Case 1: $\overline{E}$ falls before $\overline{W}$ falls

The output buffers may become enabled (reading) if $\overline{E}$ falls before $\overline{W}$ falls. $\overline{W}$ is used to disable (three-state) the outputs so input data can be applied. TWLDV must be met to allow the $\overline{W}$ signal time to disable the outputs before applying input data. Also, at the end of the cycle the outputs may become active if $\overline{W}$ rises before E. The RAM outputs will disable (three-state) after E rises (TEHQZ). In this type of write cycle TWLEL and TEHWH may be ignored.

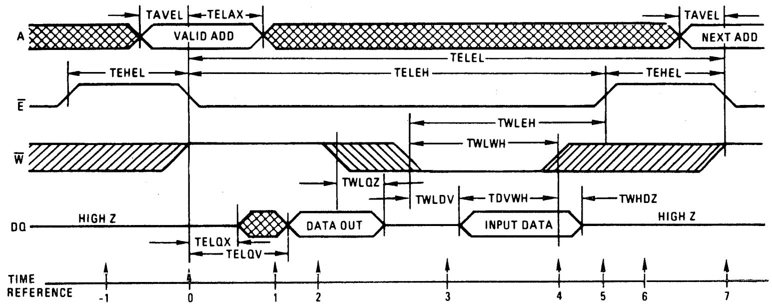
Case 2: $\overline{E}$ falls equal to or after $\overline{W}$ falls, and $\overline{E}$ rises before or equal to $\overline{W}$ rises.

This $\overline{E}$ and $\overline{W}$ control timing will guarantee that the data outputs will stay disabled throughout the cycle, thus simplifying the data input timing. TWLEL and TEHWH must be met but TWLDV becomes meaningless and can be ignored. In this cycle TDVWH and TWHDZ become TDVEH and TEHDZ. In other words, reference data setup and hold times to the $\overline{E}$ rising edge.

	IF	OBSERVE	IGNORE
Case 1	$\overline{E}$ falls before $\overline{W}$	TWLDV	TWLEL
Case 2	$\overline{E}$ falls after $\overline{W}$ & $\overline{E}$ rises before $\overline{W}$	TWLEL TEHWH	TWLDV TWHDV

If a series of consecutive write cycles are to be performed, $\overline{W}$ may be held low until all desired locations have been written (an extension of Case 2).

Read Modify Write Cycle



TRUTH TABLE

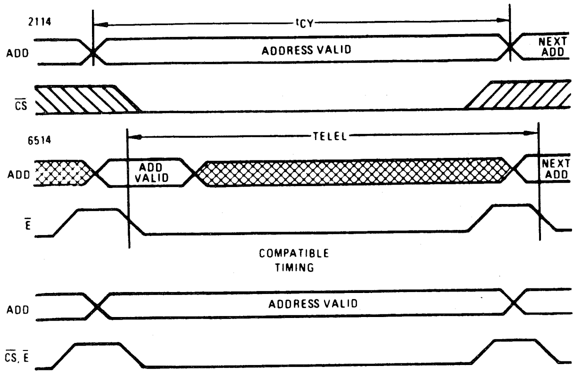
TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	DATA I/O DQ	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↓	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	READ MODE, OUTPUT ENABLED
2	L	H	X	V	READ MODE, OUTPUT VALID
3	L	L	X	Z	WRITE MODE, OUTPUT HIGH Z
4	L	↑	X	V	WRITE MODE, DATA IS WRITTEN
5	↑	H	X	Z	WRITE COMPLETED
6	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
7	↓	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

If the pulse width of $\overline{W}$ is relatively short in relation to that of $\overline{E}$ a combination read-write cycle may be performed. If $\overline{W}$ remains high for the first part of the cycle, the outputs will become active during time (T = 1). Data out will be valid during time (T = 2). After the data is read, $\overline{W}$ can go low. After minumum TWLWH, $\overline{W}$ may return high. The information just written may now be read or $\overline{E}$ may return high, disabling the output buffers and preparing the device for the next cycle. Any number or sequence of read-write operations may be performed while $\overline{E}$ is low providing all timing requirements are met.

NOTES:

In the above descriptions the numbers in parenthesis (T = n) refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

2114 Compatibility



2114 – Requires the Address to Remain Valid Throughout the Cycle.

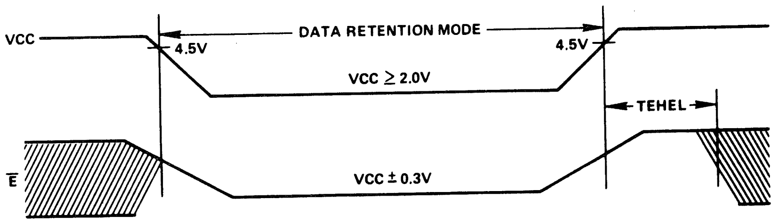
6514 – Requires Valid Address for Only a Small Portion of the Cycle, but Requires $\overline{E}$ to Fall to Initiate Each Cycle.

Low Voltage Data Retention

MHS CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC + 0.3V to VCC - 0.3V.
2. On RAMs which have selects or output enables (e.g. $\overline{S}$, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. All other inputs should be held either high (at CMOS VCC) or at ground to minimize ICCDR.
4. Inputs which are to be held high (e.g. $\overline{E}$) must be kept between VCC + 0.3V and 70% of VCC during the power up and power down transitions.
5. The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 volts).

DATA RETENTION TIMING



Ordering Information

Example: **HM 1 – 6514 – 9**

- HM: MHS MEMORY
- 1: PACKAGE
- 6514: DEVICE
- 9: VERSION/TEMP. RANGE

		TEMPERATURE RANGE		
		MILITARY	INDUSTRIAL	COMMERCIAL
PACKAGE		-2	-9	-5
CERDIP	1 –	YES	YES	YES
EPOXY	3 –	NO	YES	YES
LEADLESS	4–	YES	YES	YES

2

MHS
MATRA-HARRIS SEMICONDUCTEURS

data sheet

HM 65161
2K × 8
CMOS STATIC RAM

Features

ASYNCHRONOUS
- FAST ACCESS : 70ns max
- STAND BY CURRENT : 100 μA max
- OPERATING SUPPLY CURRENT : 60 mA max
- DATA RETENTION : 2 V min @ 40 μ A max.
- STATIC MEMORY CELL
- INDUSTRY STANDARD PIN OUT
- HIGH OUTPUT DRIVE : 5std TTL LS/load
- SINGLE SUPPLY : 5 V Vcc
- TTL COMPATIBLE INPUTS AND OUTPUTS
- WIDE TEMPERATURE RANGE
- GATED INPUT BUFFER

Description

. The HM 65161 is a 16384 bits static Random access memory organized as 2048 words by 8 bits using C MOS technology and operates from the single 5V supply.

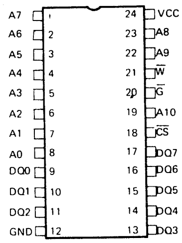
. The HM 65161 use «state of the art» MHS technology : the scaled self aligned junction isolation featuring the fastest 2Kx8 CMOS static RAM of the market : 70ns. max. Address access time.

. The HM 65161 is ideally suited for use in microprocessor based systems. The bytewide organization simplifies the memory array design. The guaranteed low voltage data retention characteristics allow easy implementation of non volatile read/write memory by using very small batteries.

. 8 product available, 100 % screened following MIL STD 883 class B.

Pinout

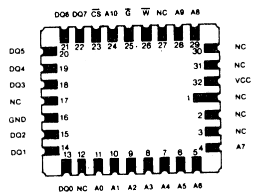
TOP VIEW



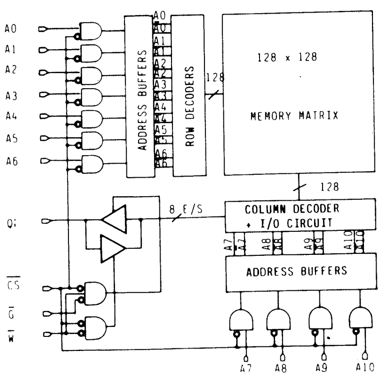
A Address input
DQ Data Input/Output
C̄S̄ Chip Select
Ḡ Output Enable
W̄ Write Enable

LCC

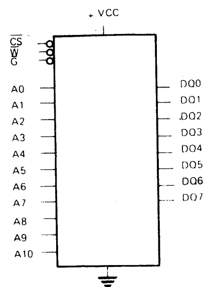
BOTTON VIEW



Functional Diagram



Logic Symbol



2

• ABSOLUTE MAXIMUM RATINGS

Supply voltage (Vcc-GND) - 0.3V* to + 7V
Input or Output Voltage Applied : (GND-0.3V*) to : (Vcc + 0.3V)
Storage temperature : 65° C to + 150° C
* IV pulse width 50 ns

• OPERATING RANGE

	Operating Voltage Range	Operating Temperature
Military (- 2)	4.5V to 5.5V	- 55° to + 125°
Industrial (- 9)	4.5V to 5.5V	- 40° to + 85°
Commercial (- 5)	4.5V to 5.5V	0° to + 70°

ELECTRICAL CHARACTERISTICS

DC PARAMETERS

SYMBOL	PARAMETER	65161-5	65161-9	65161-2	UNIT	VALUE
ICCSB (1)	standby supply current	2	3	4	mA	max
ICCSB1 (2)	standby supply current	100	350	1000	μA	max
ICCOP (3)	average operating supply current	60	65	70	mA	max
ICC (4)	power supply current	60	65	70	mA	max
II/O (5)	input/output leakage current	± 1	± 1	± 2	μA	max
VIL (6)	input low voltage	0.8	0.8	0.8	V	max
VIH (6)	input high voltage	2.4	2.4	VCC-2	V	min
VOL (7)	output low voltage	0.4	0.4	0.4	V	max
VOH (7)	output high voltage	2.4	2.4	2.4	V	min
CI (8)	input capacitance	8	8	8	PF	max
CO (8)	input/output capacitance	10	10	10	PF	max

NOTE 1 : CS = VIH ;Iio = 0 ; input gating
NOTE 2 : $\overline{CS}$ = VCC-0.3V ;Iio = 0
NOTE 3 : ICCOP with a duty cycle = 100 % ; VI = VCC or GND ; IO = 0 ; typical derating = 5 mA/MHz increase in ICCOP
NOTE 4 : $\overline{CS}$ = VIL, II/O = 0 ; addresses and data inputs level = VCC or GND
NOTE 5 : VCC = 5V ; VIN = GND to VCC
NOTE 6 : VIH max = VCC + 0.3V ; VIL min = -IV pulse width 50 ns
NOTE 7 : IOL = 4 mA ; IOH = - 1 mA
NOTE 8 : capacitance sampled and guaranteed not 100 % tested TA = 25° C, f = 1 MHz

AC PARAMETERS

AC test conditions :
- Vc = 5V ± 10 %
- Input pulse levels : OV to 3.0V
- Input and Output timing
- References levels : 1.5V
- Output load : 1 TTL gate and CL = 100 pf (including scope and jig)
- Input rise and fall times : 10 ns

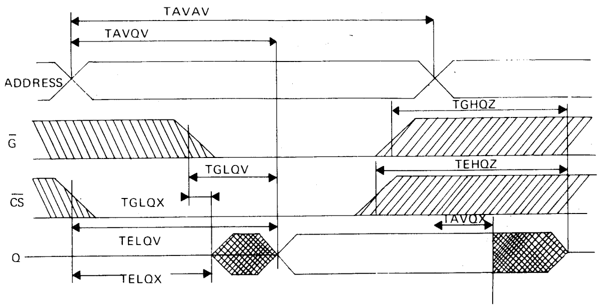
WRITE CYCLE

SYMBOL	PARAMETER (1)	65161-5	65161-9	65161-2	UNIT	VALUE
TAVAV	write cycle time	70	70	90	ns	min
TELWH*	chip selection to end of write	65	65	65	ns	min
TAVWL	address set up time	0	0	0	ns	min
TWLWH	write pulse width	65	65	65	ns	min
TWHAV	write recovery time	5	5	5	ns	min
TGHQZ	output enable to output in high Z	35	35	35	ns	max
TWLQZ	write low to output in high Z	35	35	35	ns	max
TDVWH	input data valid to write high	30	30	30	ns	min
TWHDX	data hold from write time	5	5	5	ns	min
TWHQX	output active from end of write	5	5	5	ns	min
TWLEH	write low to chip select high	65	65	85	ns	min
TDVEH	input data valid to chip select high	30	30	30	ns	min

READ CYCLE

SYMBOL	PARAMETER (1)	65161-5	65161-9	65161-2	UNIT	VALUE
TAVAV	read cycle time	70	70	90	ns	min
TAVQV	address access time	70	70	90	ns	max
TELQV	chip select access time	70	70	90	ns	max
TELQX	chip select low in active output	10	10	10	ns	min
TGLQV	output enable to output valid time	40	40	60	ns	max
TGLQX	output enable to output in low Z time	0	0	0	ns	min
TEHQZ	chip select disable time	35	35	35	ns	max
TGHQZ	output enable to output in high Z time	35	35	35	ns	max
TAVQX	output holdtime from address change	10	10	10	ns	min

1 READ CYCLE

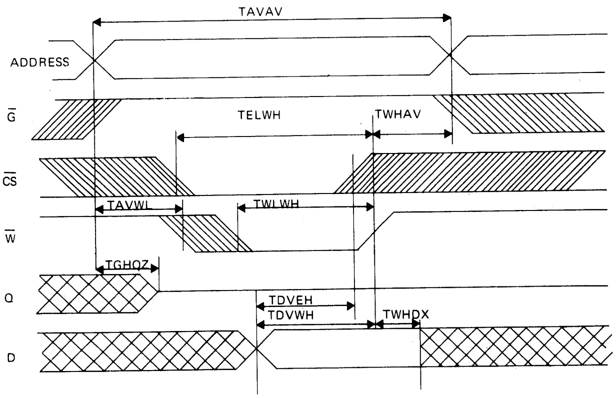


NOTE : W̅ IS HIGH FOR A READ CYCLE

TRUTH TABLE :

C̅S̅	G̅	W̅	D	Q	POWER SUPPLY CURRENT	MODE
H	X	X	Z	Z	ICCSB	C̅S̅ = VIH DESELECT
H	X	X	Z	Z	ICCSB1	C̅S̅ ≥ Vcc-0.3 DESELECT
L	L	H	Z	VALID	ICC	READ
L	H	L	VALID	Z	ICC	WRITE
L	L	L	VALID	Z	ICC	WRITE
L	H	H	Z	Z	ICC	DESELECT

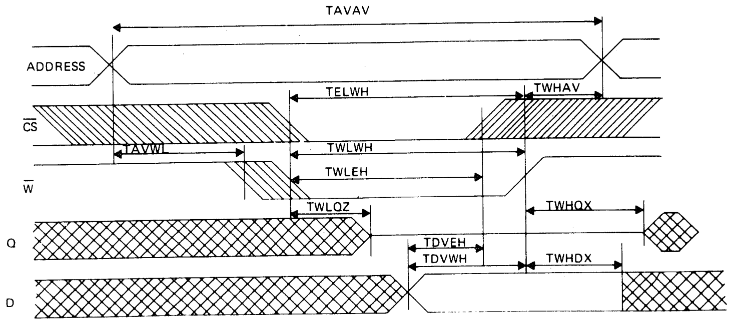
3. WRITE CYCLE TIME 1



This write cycle time is recommended for continuous writing.

G̅ = VIH during this write cycle.

3. WRITE CYCLE TIME 2



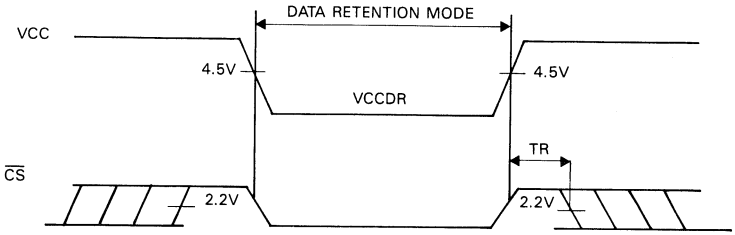
NOTE G̅ IS LOW THROUGHOUT WRITE CYCLE

This write cycle time may be used for write and read in the same cycle (write followed by read)

Data retention Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	65161 -5 min	65161 -5 max	65161 -9 min	65161 -9 max	65161 -2 min	65161 -2 max	UNIT
VCC for data retention	VCCDR	$\overline{CS}$ = VCC VIN = OV or VCC	2	–	2	–	2	–	V
data retention current	ICCDR	VCC = 2.0V, $\overline{CS}$ = VCC VIN = OV or VCC	–	40	–	140	–	400	μA
operating recovery time	TR		TAVAV		TAVAV		TAVAV		

TAVAV = read cycle time



2

Ordering Information

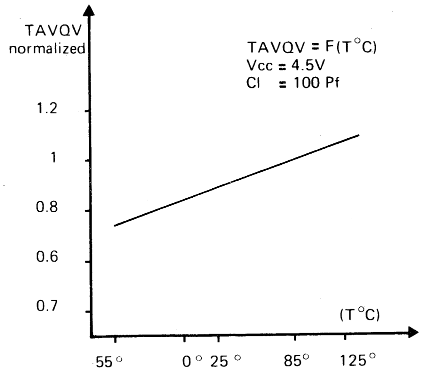
DEVICE TYPE	PACKAGE	TEMPERATURE RANGE
HM1 - 65161 -2	CERAMIC DIL	− 55° C to + 125° C
HM1 - 65161 -5	CERAMIC DIL	0° C to + 70° C
HM1 - 65161 -8	CERAMIC DIL	− 55° C to + 125° C
HM1 - 65161 -9	CERAMIC DIL	− 40° C to + 85° C
HM3 - 65161 -5	PLASTIC DIL	0° C to + 70° C
HM3 - 65161 -9	PLASTIC DIL	− 40° C to + 85° C
HM4 - 65161 -5	L.C.C.	0° C to + 70° C
HM4 - 65161 -8	L.C.C.	− 55° C to + 125° C
HM4 - 65161 -9	L.C.C.	− 40° C to + 85° C

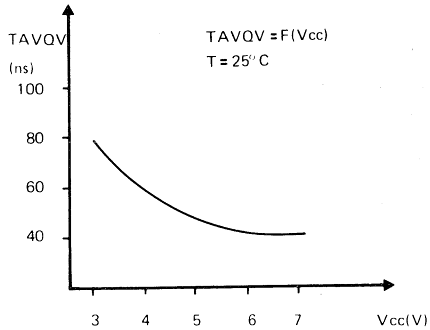
TEMPERATURE RANGE (-5, 2, -8, -9)

DEVICE TYPE

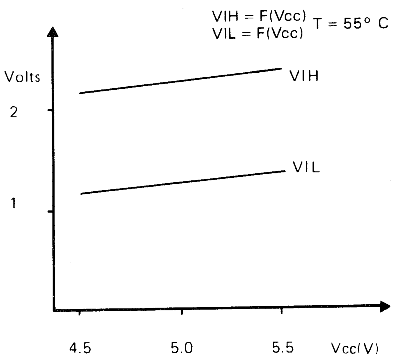
PACKAGE (1, 3, 4)

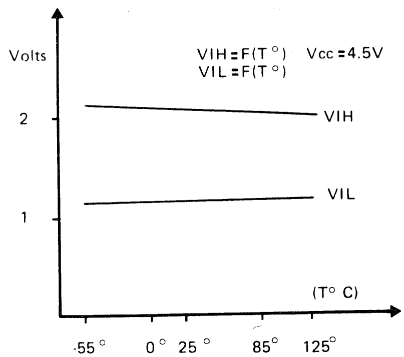
READ CYCLE TIME



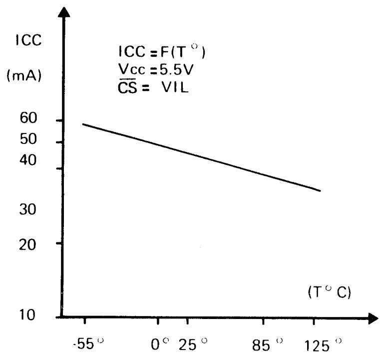


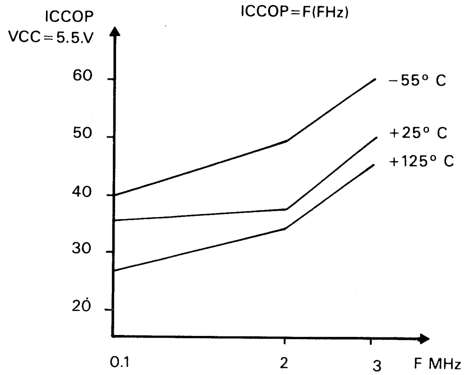
INPUT VOLTAGE





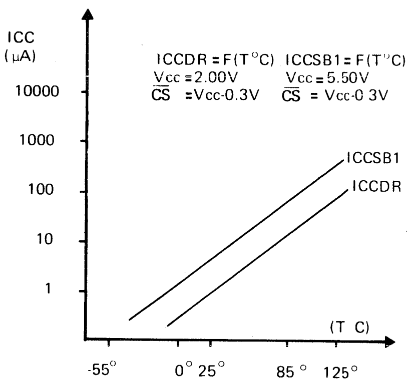
POWER SUPPLY CURRENT

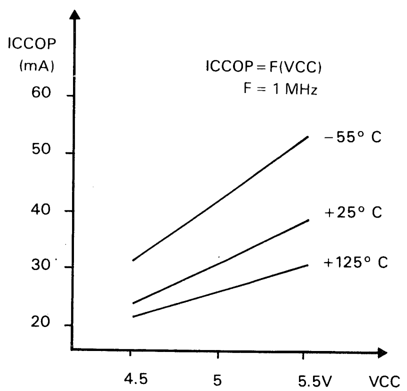




2

STANDBY AND DATA RETENTION CURRENT





MHS
MATRA-HARRIS SEMICONDUCTEURS

data sheet

HM 65261
16K × 1
CMOS STATIC RAM

PRELIMINARY

Features

- . ASYNCHRONOUS
- . FAST ACCESS : 70 ns max
- . STAND BY CURRENT : 50 μa max
- . OPERATING SUPPLY CURRENT : 50 mA
- . DATA RETENTION : 2 V min @ 20 μA max
- . STATIC OPERATION : NO CLOCKS OR REFRESH REQUIRED
- . INDUSTRY STANDARD PIN OUT
- . GATED INPUT BUFFER
- . WIDE TEMPERATURE RANGE SPEC's : - 55°C to + 125°C
- . SINGLE SUPPLY : 5 V

Description

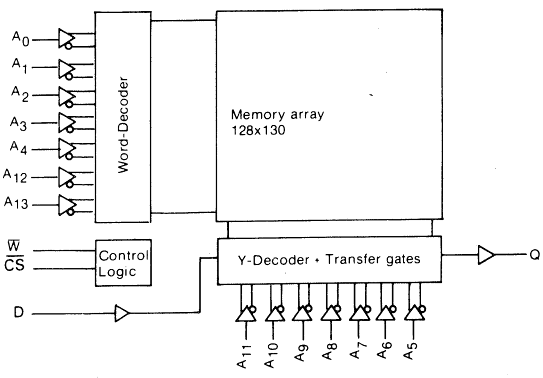
. The HM 65261 is a 16384 bits Statics Random Access Memory organised as 16384 words by 1 bit using CMOS technology and operates from the single 5V supply.

. The HM 65261 uses "state of the art" MHS technology : the scaled Self Aligned Junction Isolation featuring low stand by current and fast address access time.

. The HM 65261 features fully static operation requiring no external clocks or timing strobes, equal access and cycle times. The pin out is the JEDEC 20 pin. 300" width package allowing maximum board packing density.

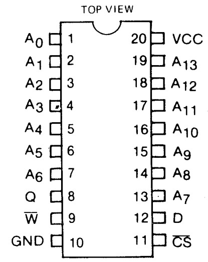
. 8 product available, 100 % screened following MIL STD 883 class B.

Functional Diagram



Pinouts

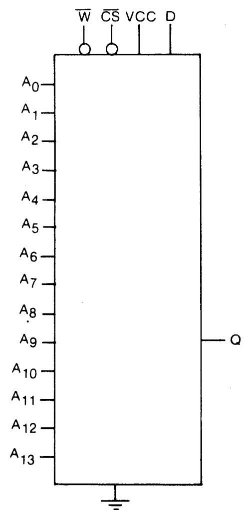
Pinout



A-Address input
Q-Data output
D-Data in
$\overline{CS}$-Chip Select
$\overline{W}$-Write enable

2

Logic Symbol



• ABSOLUTE MAXIMUM RATINGS

Supply voltage (VCC-GND) -1V* to 7V
Input or output voltage applied : GND-1V* VCC+0.3V
Storage temperature : 65° C to + 150° C
* Pulse width 50 ns

• OPERATING RANGE

	Operating Voltage	Operating Temperature
Military - 2	VCC ± 10 %	- 55° C to + 125° C
Industrial - 9	VCC ± 10 %	- 40° C to + 85° C
Commercial - 5	VCC ± 10 %	0° C to + 70° C

ELECTRICAL CHARACTERISTICS

DC PARAMETERS

SYMBOL	PARAMETERS	65261-5	65261-9	65261-2	UNIT	VALUE
ICCSB (1)	standby supply current	3	4	4	mA	max
ICCSB1 (2)	standby supply current	50	400	900	μA	max
ICCOP (3)	average operating supply current	50	50	50	mA	max
ICC (4)	power supply current	50	50	50	mA	max
II/O (5)	input/output leakage current	± 2	± 2	± 5	μA	max
VIL (6)	input low voltage	0.8	0.8	0.8	V	max
VIH (6)	input high voltage	2.2	2.2	2.2	V	min
VOL (7)	output low voltage	0.4	0.4	0.4	V	max
VOH (7)	output high voltage	2.4	2.4	2.4	V	min
CI (8)	input capacitance	8	8	8	pf	max
CO (8)	input/output capacitance	10	10	10	pf	max

NOTE 1 : CS = VIH ;Iio = 0 ; input gating
NOTE 2 : $\overline{CS}$ = VCC-0.3V ;Iio = 0
NOTE 3 : ICCOP with a duty cycle = 100 % ; VI = VCC or GND ; IO = 0 ; typical derating = 2 mA/MHz increase in ICCOP
NOTE 4 : $\overline{CS}$ = VIL, II/O = 0 ; addresses and data inputs level = VCC or GND
NOTE 5 : VCC = 5.5V ; VIN = GND to VCC
NOTE 6 : VIH max = VCC + 0.3V ; VIL min = -IV pulse width 50 ns
NOTE 7 : IOL = 16 mA ; IOH = − 1 mA
NOTE 8 : capacitance sampled and guaranteed not 100 % tested TA = 25° C, f = 1 MHz

2

AC PARAMETERS

Conditions :		
	Input pulse levels	GND to 3.0V
	Input rise and fall times	5 ns
	Input timing reference levels	1.5V
	Output reference levels	1.5V
	Output load	(see figure 1)

WRITE CYCLE

SYMBOL	PARAMETERS	65261-5	65261-9	65261-2	UNIT	VALUE
TAVAV	write cycle time	70	70	85	ns	min
TELWH	chip selection to end of write	55	55	65	ns	min
TAVWH	address valid to end of write	50	50	60	ns	min
TAVWL	address set up time	0	0	0	ns	min
TWLWH	write pulse width	50	50	55	ns	min
TWHAV	write recovery time	0	0	0	ns	min
TDVWH	input data valid to write high	30	30	35	ns	min
TWHDX	data hold from write time	0	0	0	ns	min
TWLQZ	write enable to output in high	30	30	40	ns	max
TWHQX	output active to end of write	0	0	0	ns	min

READ CYCLE

TAVAV	read cycle time	70	70	85	ns	min
TAVQV	address access time	70	70	85	ns	max
TAVQX	output holdtime from address change	5	5	5	ns	min
TELQV	chip select access time	70	70	85	ns	max
TELQX	chip selection to output in low Z	5	5	5	ns	min
TEHQZ	chip enable output disable time	30	30	40	ns	max
TELIC	chip selection to power up time	0	0	0	ns	min
TEHICCL	chip deselection to power downtime	35	35	40	ns	max

• ABSOLUTE MAXIMUM RATINGS

Supply voltage (VCC-GND) -1V* to 7V
Input or output voltage applied : GND-1V* VCC+0.3V
Storage temperature : 65° C to + 150° C
* Pulse width 50 ns

• OPERATING RANGE

	Operating Voltage	Operating Temperature
Military - 2	VCC ± 10 %	- 55° C to + 125° C
Industrial - 9	VCC ± 10 %	- 40° C to + 85° C
Commercial - 5	VCC ± 10 %	0° C to + 70° C

ELECTRICAL CHARACTERISTICS

DC PARAMETERS

SYMBOL	PARAMETER	65261C-5	65261C-9	65261C-2	UNIT	VALUE
ICCSB (1)	standby supply current	4	5	5	mA	max
ICCSB1 (2)	standby supply current	2000	3000	4000	μA	max
ICCOP (3)	average operating supply current	60	60	60	mA	max
ICC (4)	power supply current	60	60	60	mA	max
II/O 5)	input/output leakage current	± 2	± 5	± 10	μA	max
VIL (6)	input low voltage	0.8	0.8	0.8	V	max
VIH (6)	input high voltage	2.2	2.2	2.2	V	min
VOL (7)	output low voltage	0.4	0.4	0.4	V	max
VOH (7)	output high voltage	2.4	2.4	2.4	V	min
CI (8)	input capacitance	8	8	8	pf	max
CO (8)	input/output capacitance	10	10	10	pf	max

NOTE 1 : CS = VIH ;Iio = 0 ; input gating
NOTE 2 : $\overline{CS}$ = VCC-0.3V ;Iio = 0
NOTE 3 : ICCOP with a duty cycle = 100 % ; VI = VCC or GND ; IO = 0 ; typical derating = 2 mA/MHz increase in ICCOP
NOTE 4 : $\overline{CS}$ = VIL, II/O = 0 ; addresses and data inputs level = VCC or GND
NOTE 5 : VCC = 5.5V ; VIN = GND to VCC
NOTE 6 : VIH max = VCC + 0.3V ; VIL min = -IV pulse width 50 ns
NOTE 7 : IOL = 16 mA ; IOH = − 1 mA
NOTE 8 : capacitance sampled and guaranteed not 100 % tested TA = 25° C, f = 1 MHz

2

AC PARAMETERS

Conditions :	
Input pulse levels	GND to 3.0V
Input rise and fall times	5 ns
Input timing refe:ence levels	1.5V
Output reference levels	1.5V
Output load	(see figure 1)

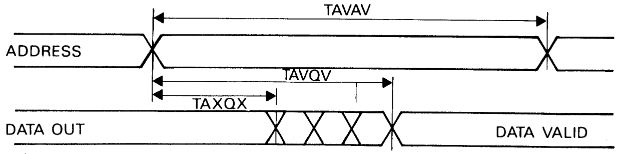
WRITE CYCLE

SYMBOL	PARAMETERS	65261C-5	65261C-9	65261C-2	UNIT	VALUE
TAVAV	write cycle time	85	85	100	ns	min
TELWH	chip selection to end of write	65	65	80	ns	min
TAVWH	address valid to end of write	60	60	75	ns	min
TAVWL	address set up time	0	0	0	ns	min
TWLWH	write pulse width	55	55	60	ns	min
TWHAV	write recovery time	0	0	0	ns	min
TDVWH	input data valid to write high	35	35	40	ns	min
TWHDX	data hold from write time	0	0	0	ns	min
TWLQZ	write enable to output in high	40	40	40	ns	max
TWHQX	output active to end of write	0	0	0	ns	min

READ CYCLE

TAVAV	read cycle time	85	85	100	ns	min
TAVQV	address access time	85	85	100	ns	max
TAVQX	output holdtime from address change	5	5	5	ns	min
TELQV	chip select access time	85	85	100	ns	max
TELQX	chip selection to output in low Z	5	5	5	ns	min
TEHQZ	chip enable output disable time	40	40	40	ns	max
TELIC	chip selection to power up time	0	0	0	ns	min
TEHICCL	chip deselection to power downtime	40	40	45	ns	max

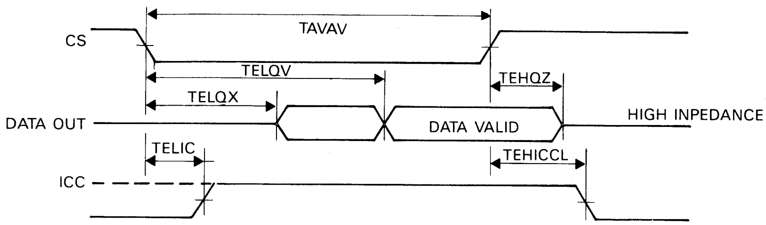
READ CYCLE N° 1 (1, 2)



TRUTH TABLE

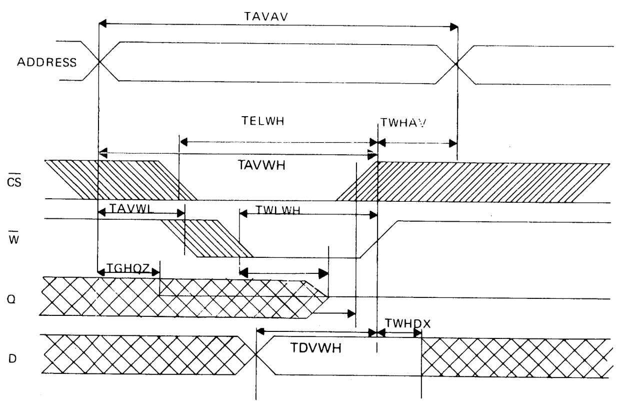
CS	W	Q	Power Supply Current	Mode
H	X	Z	ICCSB	$\overline{CS}$ = VIH deselect
H	X	Z	ICCSB1	$\overline{CS} \geqslant$ VCC-0.3V deselect
L	H	valid	ICC	Read
L	L	Z	ICC	Write

READ CYCLE N° 2 (1, 3)



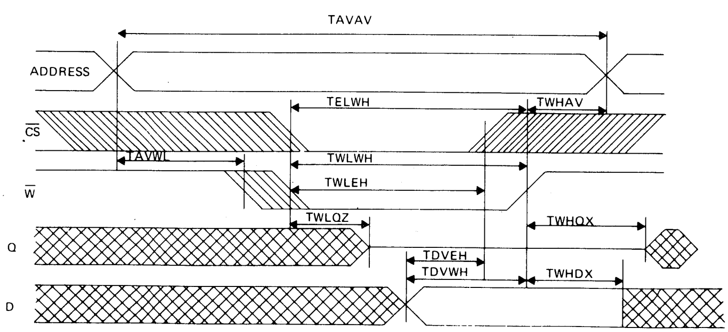
1) $\overline{WE}$ is high for read cycle
2) $\overline{CS}$ is low for read cycle
3) Address valid prior to or coincident with CS transition bw

3. WRITE CYCLE TIME ($\overline{CS}$ controlled)



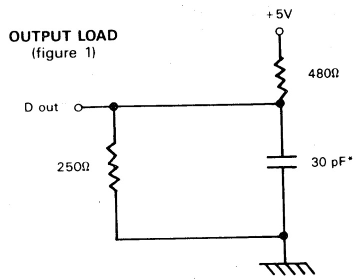
2

3. WRITE CYCLE TIME ($\overline{WE}$ controlled)



$\overline{CS}$ or $\overline{WE}$ must be high during address transitions

OUTPUT LOAD
(figure 1)

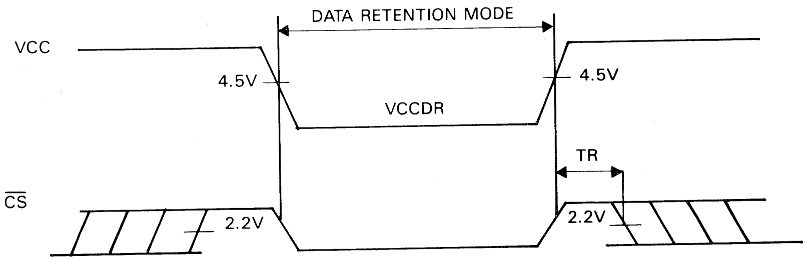


* including scope and jig

Data retention Characteristics (only for 65261)

PARAMETER	SYMBOL	TEST CONDITIONS	65261 -5	65261 -9	65261 -2	UNIT	VALUE
VCC for data retention	VCCDR	$\overline{CS}$ = VCC VIN = OV or VCC	2	2	2	V	min
data retention current	ICCDR	VCC = 2.0V, $\overline{CS}$ = VCC VIN = OV or VCC	20	200	300	μA	max
operating recovery time	TR		TAVAV	TAVAV	TAVAV	ns	min

TAVAV = read cycle time



Ordering Information

DEVICE TYPE	PACKAGE	TEMPERATURE RANGE
HM1 - 65261 (C) -5	CERAMIC DIL	0° C to + 70° C
HM1 - 65261 (C) -9	CERAMIC DIL	-40° C to + 85° C
HM1 - 65261 (C) -2	CERAMIC DIL	-55° C to +125° C
HM1 - 65261 (C) -8	CERAMIC DIL	-55° C to +125° C
HM3 - 65261 (C) -5	PLASTIC DIL	0° C to + 70° C
HM3 - 65261 (C) -9	PLASTIC DIL	-40° C to + 85° C

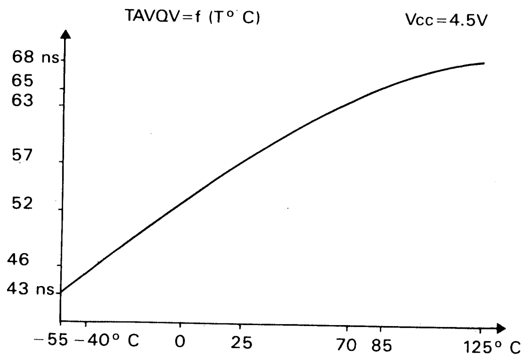
TEMPERATURE RANGE (-5, -9, -2)

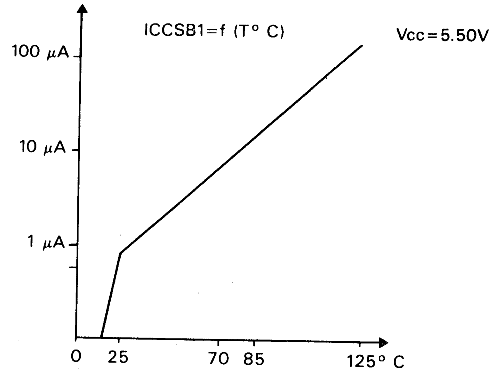
Blank : Standard
C Low speed] DEVICE TYPE

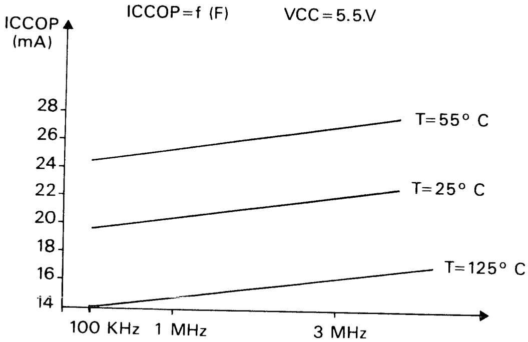
PACKAGE (1, 3)

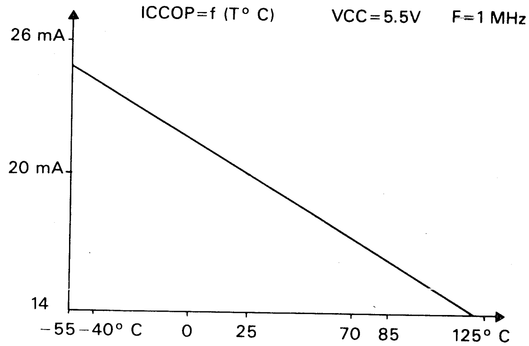
LCC 20 pins will be available end of 1983

2

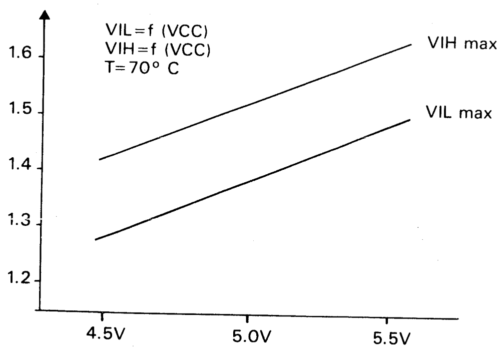

TAVQV=f (T° C)
Vcc=4.5V
68 ns
65
63
57
52
46
43 ns
−55 −40° C
0
25
70
85
125° C

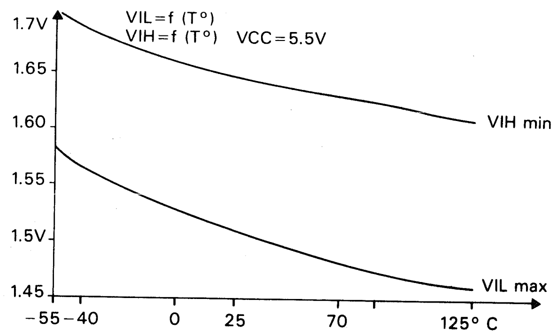

ICCSB1=f (T° C)
Vcc=5.50V
100 μA
10 μA
1 μA
0
25
70
85
125° C


ICCOP
(mA)
ICCOP=f (F)
VCC=5.5V
28
26
24
22
20
18
16
14
T=55° C
T=25° C
T=125° C
100 KHz
1 MHz
3 MHz


ICCOP=f (T° C)
VCC=5.5V
F=1 MHz
26 mA
20 mA
14
−55 −40° C
0
25
70
85
125° C

2


VIL=f (VCC)
VIH=f (VCC)
T=70° C
VIH max
VIL max
1.6
1.5
1.4
1.3
1.2
4.5V
5.0V
5.5V


VIL=f (T°)
VIH=f (T°)
VCC=5.5V
1.7V
1.65
1.60
1.55
1.5V
1.45
VIH min
VIL max
−55 −40
0
25
70
125° C

MATRA-HARRIS SEMICONDUCTEURS

data sheet

HM-6561
MM3-S0001
256 × 4 CMOS RAM

Features

. LOW STANDBY POWER	50 uW max
. LOW OPERATING POWER	20 mW/MHz max
. FAST ACCESS TIME	220 nsec max
. DATA RETENTION VOLTAGE	2.0 volts min

- . TTL COMPATIBLE INPUT/OUTPUT
- . MM3-S0001 LOW CONSUMPTION VERSION
- . ON CHIP ADDRESS REGISTERS
- . COMMON DATA INPUT/OUTPUT
- . THREE STATE OUTPUTS
- . MM3-S0001 SUPPLY VOLTAGE 2.8 V min
- . MILITARY TEMPERATURE RANGE
- . INDUSTRIAL TEMPERATURE RANGE

Description

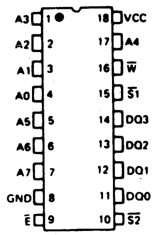
The HM-6561 and MM3-S0001 are 256 by 4 static CMOS RAMs fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays. The data inputs and outputs are multiplexed internally for common I/O bus compatibility.

The HM-6561 and MM3-S0001 are fully static RAMs and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature. The MM3-S0001 is developped for low consumption applications. This product is assembled in an 18 pin Plastic Cerdip Package.

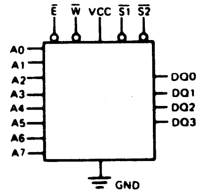
Pinout

TOP VIEW



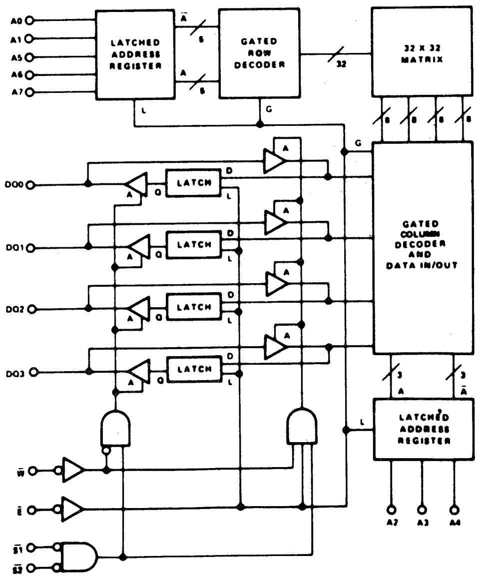
A – Address Input
E̅ – Chip Enable
S̅ – Chip Select
W̅ – Write Enable
DQ – Data In/Out

Logic Symbol



2

Functional Diagram



ALL LINES POSITIVE LOGIC - ACTIVE HIGH

THREE STATE BUFFERS
A HIGH → OUTPUT ACTIVE

DATA LATCHES
L HIGH → Q = D
Q LATCHES ON FALLING EDGE OF L

ADDRESS LATCHES AND GATED DECODERS
LATCH ON RISING EDGE OF L
GATE ON RISING EDGE OF G

CAUTION: These devices are sensitive to electrostatic discharge

ABSOLUTE MAXIMUM RATINGS

Supply Voltage - (VCC - GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10	0.1	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10	0.01	μA	VCC = 2.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤VIO≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.2	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		4.5	V	IO = -0.4mA
	CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10	6	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		220	120	ns	④
	TAVQV	Address Access Time		220	110	ns	④
	TSLQX	Chip Select Output Enable Time	20	120	50	ns	④
	TWLQZ	Write Enable Output Disable Time		120	50	ns	④
	TSHQZ	Chip Select Output Disable Time		120	50	ns	④
	TELEH	Chip Enable Pulse Negative Width	220		120	ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		50	ns	④
	TAVEL	Address Setup Time	0		-10	ns	④
	TELAX	Address Hold Time	40		20	ns	④
	TDVWH	Data Setup Time	100		50	ns	④
	TWHDX	Data Hold Time	0		0	ns	④
	TWLDV	Write Data Delay Time	120		50	ns	④
	TWLSH	Chip Select Write Pulse Setup Time	120		60	ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	120		60	ns	④
	TSLWH	Chip Select Write Pulse Hold Time	120		60	ns	④
	TELWH	Chip Enable Write Pulse Hold Time	120		60	ns	④
	TWLWH	Write Enable Pulse Width	120		60	ns	④
	TWLSL	Early Output High Z Time	0		-10	ns	④
	TSHWH	Late Output High Z Time	0		-10	ns	④
	TELEL	Read or Write Cycle Time	320		170	ns	④

NOTES:
① All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
③ Capacitance sampled and guaranteed – not 100% tested.
④ AC Test Conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.

2

ABSOLUTE MAXIMUM RATINGS

Supply Voltage - (VCC - GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	TEMP. = 25°C ① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10	0.1	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10	0.01	μA	VCC = 2.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ⩽ VI ⩽ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	0.0	μA	GND ⩽ VIO ⩽ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.2	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		4.5	V	IO = -0.4mA
	CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10	6	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300	160	ns	④
	TAVQV	Address Access Time		300	150	ns	④
	TSLQX	Chip Select Output Enable Time	20	150	60	ns	④
	TWLQZ	Write Enable Output Disable Time		150	60	ns	④
	TSHQZ	Chip Select Output Disable Time		150	60	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		160	ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		50	ns	④
	TAVEL	Address Setup Time	0		-10	ns	④
	TELAX	Address Hold Time	50		30	ns	④
	TDVWH	Data Setup Time	150		100	ns	④
	TWHDX	Data Hold Time	0		0	ns	④
	TWLDV	Write Data Delay Time	150		60	ns	④
	TWLSH	Chip Select Write Pulse Setup Time	180		120	ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	180		120	ns	④
	TSLWH	Chip Select Write Pulse Hold Time	180		120	ns	④
	TELWH	Chip Enable Write Pulse Hold Time	180		120	ns	④
	TWLWH	Write Enable Pulse Width	180		120	ns	④
	TWLSL	Early Output High Z Time	0		-10	ns	④
	TSHWH	Late Output High Z Time	0		-10	ns	④
	TELEL	Read or Write Cycle Time	400		210	ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC Test Conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.

2

ABSOLUTE MAXIMUM RATINGS

Supply Voltage - (VCC - GND)	-0.3V to +8.0V
Applied Input or Output Voltage	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC Commercial	4.5V to 5.5V
Operating Temperature Commercial	0°C to 75°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	TEMP. = 25°C ① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100	10	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		100	1	μA	VCC = 2.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0			V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤VIO≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.2	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		4.5	V	IO = -0.2mA
	CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10	6	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		350	200	ns	④
	TAVQV	Address Access Time		360	200	ns	④
	TSLQX	Chip Select Output Enable Time	20	180	80	ns	④
	TWLQZ	Write Enable Output Disable Time		180	80	ns	④
	TSHQZ	Chip Select Output Disable Time		180	80	ns	④
	TELEH	Chip Enable Pulse Negative Width	350		200	ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		90	ns	④
	TAVEL	Address Setup Time	10		0	ns	④
	TELAX	Address Hold Time	70		40	ns	④
	TDVWH	Data Setup Time	170		120	ns	④
	TWHDX	Data Hold Time	0		0	ns	④
	TWLDV	Write Data Delay Time	200		60	ns	④
	TWLSH	Chip Select Write Pulse Setup Time	210		150	ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	210		150	ns	④
	TSLWH	Chip Select Write Pulse Hold Time	210		150	ns	④
	TELWH	Chip Enable Write Pulse Hold Time	210		150	ns	④
	TWLWH	Write Enable Pulse Width	210		150	ns	④
	TWLSL	Early Output High Z Time	0		-10	ns	④
	TSHWH	Late Output High Z Time	0		-10	ns	④
	TELEL	Read or Write Cycle Time	500		290	ns	④

NOTES:
① All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
③ Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage - (VCC - GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC	2.8V to 5.8V
Operating Temperature	-20°Cto+70°C

ELECTRICAL CHARACTERISTICS

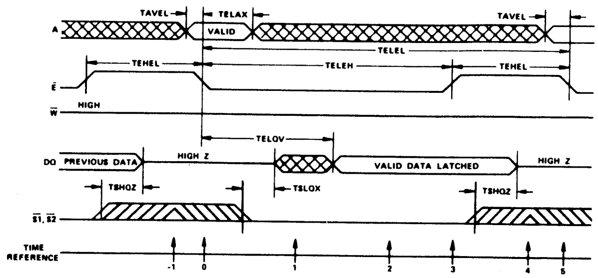
	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 3.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10	0.1	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		300	10,00	µA	f = 1 KHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10		µA	VCC = 2.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0			V	
	II	Input Leakage Current	-1.0	+1.0		µA	GND ⩽ VI ⩽ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0		µA	GND ⩽VIO⩽ VCC
	VIL	Input Low Voltage	-0.3	0,5		V	
	VIH	Input High Voltage	VCC-0,8	VCC-0.3		V	
	VOL	Output Low Voltage		0,5		V	IO = 20 µA
	VOH	Output High Voltage	VCC-0,5			V	IO = 50 µA
	CI	Input Capacitance ③		6		pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10		pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		750		ns	④
	TAVQV	Address Access Time		750		ns	④
	TSLQX	Chip Select Output Enable Time	20	300		ns	④
	TWLQZ	Write Enable Output Disable Time		300		ns	④
	TSHQZ	Chip Select Output Disable Time		300		ns	④
	TELEH	Chip Enable Pulse Negative Width	750			ns	④
	TEHEL	Chip Enable Pulse Positive Width	250			ns	④
	TAVEL	Address Setup Time	0			ns	④
	TELAX	Address Hold Time	100			ns	④
	TDVWH	Data Setup Time	350			ns	④
	TWHDX	Data Hold Time	0			ns	④
	TWLDV	Write Data Delay Time	400			ns	④
	TWLSH	Chip Select Write Pulse Setup Time	400			ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	400			ns	④
	TSLWH	Chip Select Write Pulse Hold Time	400			ns	④
	TELWH	Chip Enable Write Pulse Hold Time	400			ns	④
	TWLWH	Write Enable Pulse Width	400			ns	④
	TWLSL	Early Output High Z Time	0			ns	④
	TSHWH	Late Output High Z Time	0			ns	④
	TELEL	Read or Write Cycle Time	1000			ns	④

NOTES:
① All devices tested at worst case limits. Room temp. V data provided for information – not guaranteed.
② Operating Supply Current (ICCOP) is proportional to Operating Frequency.
③ Capacitance sampled and guaranteed – not 100% tested.
④ AC Test Conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – CLOAD = 50pF. All timing measurements at (VCC-VSS) reference level

2

2

Read Cycle



TRUTH TABLE

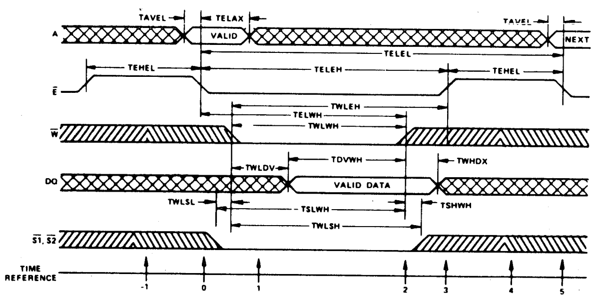
TIME REFERENCE	INPUTS $\overline{E}$	$\overline{S1}$	$\overline{W}$	A	OUTPUT DQ	FUNCTION
-1	H	H	X	X	Z	MEMORY DISABLED
0	↘	X	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	H	X	X	OUTPUT ENABLED
2	L	L	H	X	V	OUTPUT VALID
3	↗	L	H	X	V	OUTPUT LATCHED
4	H	H	X	X	Z	DEVICE DISABLED, PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

NOTES: 1) Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

The HM-6561 Read Cycle is initiated on the falling edge of $\overline{E}$. This signal latches the input address word into on chip registers. Minimum address setup and hold times must be met. After the required hold time, the address lines may change state without affecting device operation. In order to read the output data $\overline{E}$, $\overline{S1}$ and $\overline{S2}$ must be low and $\overline{W}$ must be high. The output data will be valid at access time (TELQV).

The HM-6561 has output data latches that are controlled by $\overline{E}$. On the rising edge of $\overline{E}$ the present data is latched and remains latched until $\overline{E}$ falls. Either or both $\overline{S1}$ or $\overline{S2}$ may be used to force the output buffers into a high impedance state.

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{S1}$	$\overline{W}$	A	DQ	FUNCTION
-1	H	H	X	X	X	MEMORY DISABLED
0	↘	X	X	V	X	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	L	X	X	WRITE PERIOD BEGINS
2	L	L	↗	X	V	DATA IN IS WRITTEN
3	↗	X	H	X	X	WRITE IS COMPLETED
4	H	H	X	X	X	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	X	V	X	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

NOTES: 1) Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

The write cycle begins with the $\overline{E}$ falling edge latching the address. The write portion of the cycle is defined by $\overline{E}$, $\overline{S1}$, $\overline{S2}$ and $\overline{W}$ all being low simultaneously. The write portion of the cycle is terminated by the first rising edge of any control line, $\overline{E}$, $\overline{S1}$, $\overline{S2}$ or $\overline{W}$. The data setup and data hold times (TDVWH and TWHDX) must be referenced to the terminating signal. For example, if $\overline{S2}$ rises first, data setup and hold times become TDVS2H and TS2HDX; and are numerically equal to TDVWH and TWHDX.

Data input/output multiplexing is controlled by $\overline{W}$. Care must be taken to avoid data bus conflicts, where the RAM outputs become enabled when another device is driving the data inputs. The following two examples illustrate the timing required to avoid bus conflicts.

Case 1: Both $\overline{S1}$ and $\overline{S2}$ fall before $\overline{W}$ falls.

If both selects fall before $\overline{W}$ falls, the RAM outputs will become enabled. $\overline{W}$ is used to disable the outputs, so a disable time (TWLQZ = TWLDV) must pass before any other device can begin to drive the data inputs. This method of operation requires a wider write pulse, because TWLDV + TDVWH is greater than TWLWH. In this case TWLSL and TSHWH are meaningless and can be ignored.

Case 2: $\overline{W}$ falls before both $\overline{S1}$ and $\overline{S2}$ fall.

If one or both selects are high until $\overline{W}$ falls the outputs are guaranteed not to enable at the beginning of the cycle. This eliminates the concern for data bus conflicts and simplifies data input timing. Data input may be applied as early as convenient, and TWLDV is ignored. Since $\overline{W}$ is not used to disable the outputs it can be shorter than in case 1; TWLWH is the minimum write pulse. At the end of the write period, if $\overline{W}$ rises before either select the outputs will enable, reading the data just written. They will not disable until either select goes high (TSHQZ).

	IF	OBSERVE	IGNORE
Case 1	Both $\overline{S1}$ and $\overline{S2}$ = low before $\overline{W}$ = low	TWLQZ TWLDV TDVWH	TWLWH TWLSL TSHWH
Case 2	$\overline{W}$ = low before both $\overline{S1}$ and $\overline{S2}$ = low	TWLWH TDVWH TWLSL TSHWH	TWLQZ TWLDV

If a series of consecutive write cycles are to be performed, $\overline{W}$ may remain low until all desired locations are written. This is an extension of Case 2.

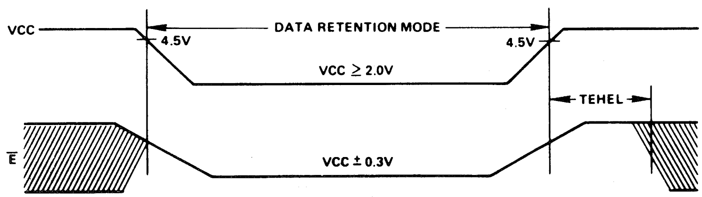
Read-Modify-Write cycles and Read-Write-Read cycles can be performed (extension of Case 1). In fact, data may be modified as many times as desired with $\overline{E}$ remaining low.

Low Voltage Data Retention

MHS CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC + 0.3V to VCC - 0.3V.
2. On RAMs which have selects or output enables (e.g. $\overline{S}$, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. All other inputs should be held either high (at CMOS VCC) or at ground to minimize ICCDR.
4. Inputs which are to be held high (e.g. $\overline{E}$) must be kept between VCC + 0.3V and 70% of VCC during the power up and power down transitions.
5. The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 volts).

DATA RETENTION TIMING



MHS
MATRA·HARRIS SEMICONDUCTEURS

data sheet

HM5-6564
8K × 8, 16K × 4 CMOS RAM

Features

• LOW POWER STANDBY	4mW MAX
• LOW POWER OPERATION	280mW/MHz MAX
• DATA RETENTION	2.0V MIN
• TTL COMPATIBLE IN/OUT	
• THREE STATE OUTPUTS	
• FAST ACCESS TIME	350ns MAX
• FULL MILITARY TEMPERATURE AVAILABLE	-55°C to 125°C
• INDUSTRIAL TEMPERATURE STANDARD	-40°C to 85°C
• COMMERCIAL TEMPERATURE AVAILABLE	0°C to 75°C
• ON CHIP ADDRESS REGISTERS	
• ORGANIZABLE 8K x 8 or 16K x 4	
• 40 PIN DIP PINOUT - 2.000" x 0.900"	

Description

The HM-6564 is a 64K bit CMOS RAM. It consists of 16 HM4-6504 4K x 1 CMOS RAMs, in leadless carriers, mounted on a ceramic substrate. The HM-6564 is configured as an extra wide, standard length 40 pin DIP. The memory appears to the system as an array of 16 4K x 1 static RAMs. The array is organized as two 8K by 4 blocks of RAM sharing only the address bus. The data inputs, data outputs, chip enables and write enables are separate for each block of RAM. This allows the user to organize the HM-6564 RAM as either an 8K by 8 or a 16K by 4 array. The HM-6564 also contains decoupling capacitors to reduce noise and to minimize the need for additional external decoupling.

This 64K memory provides a unique blend of low power CMOS semiconductor technology and advanced packaging techniques. The HM-6564 is intended for use in any application where a large amount of RAM is needed, and where power consumption and board space are prime concerns. The guaranteed low voltage data retention characteristics allow easy implementation of non-volatile read/write memory by using very small batteries mounted directly on the memory circuit board. Example applications include digital avionic instrumentation, remote data acquisition, and portable or hand held digital communications devices.

Pinout

TOP VIEW

Signal	Pin	Pin	Signal
*GND	1	40	VCC*
Q4	2	39	Q0
D4	3	38	D0
Q5	4	37	Q1
D5	5	36	D1
A0	6	35	A11
A1	7	34	A10
A2	8	33	A9
$\overline{E3}$	9	32	$\overline{E1}$
*$\overline{W2}$	10	31	$\overline{W1}$
$\overline{W2}$	11	30	$\overline{W1}$*
$\overline{E4}$	12	29	$\overline{E2}$
A6	13	28	A5
A7	14	27	A4
A8	15	26	A3
D6	16	25	D2
Q6	17	24	Q2
D7	18	23	D3
Q7	19	22	Q3
*VCC	20	21	GND*

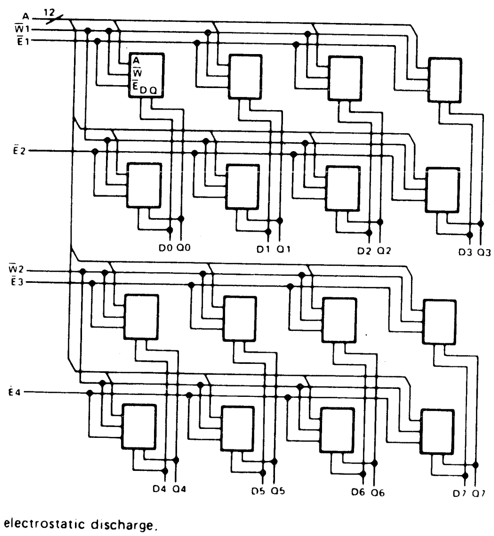
H210388 HMS 6564

*NOTES:

Pins 20 and 40 (VCC) are internally connected. Similarly pins 1 and 21 (Ground) are connected. The user is advised to connect all four VCC pins and Ground pins to his board busses. This will improve power distribution across the array and will enhance decoupling.

Pin 10 is internally connected to pin 11, and pin 30 is connected to pin 31. For those users wishing to preserve board compatibility with possible future RAM arrays, we recommend connections to the write lines be made at pins 11 and 31, leaving pins 10 and 30 free for future expansion.

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge.

2

Organization Guide

To Organize 8K x 8:

Connect:	$\overline{E}1$ with $\overline{E}3$	(Pins 9 + 32)
	$\overline{E}2$ with $\overline{E}4$	(Pins 12 + 29)
	$\overline{W}1$ with $\overline{W}2$	(Pins 11 +31)

To Organize 16K x 4:

Connect:	Q0 with Q4	(Pins 2 + 39)
	D0 with D4	(Pins 3 + 38)
	Q1 with Q5	(Pins 4 + 37)
	D1 with D5	(Pins 5 + 36)
	D2 with D6	(Pins 16 +25)
	Q2 with Q6	(Pins 17 + 24)
	D3 with D7	(Pins 18 + 23)
	Q3 with Q7	(Pins 19 + 22)
Optional	$\overline{W}1$ may be common with $\overline{W}2$	(Pins 11 + 31)

Concerns for Proper Operation of Chip Enables:

The transition between blocks of RAM requires a change in the chip enable being used. When operating in the 8K x 8 mode, use the chip enables as if there were only two, $\overline{E}1$ and $\overline{E}2$. In the 16K x 4 mode, all chip enables must be treated separately. Transitions between chip enables must be treated with the same timing constraints that apply to any one chip enable. All chip enables must be high at least one chip enable high time (TEHEL) before any chip enable can fall. More than one chip enable low simultaneously, for devices whose outputs are tied common either internally or externally, is an illegal input condition and must be avoided.

Printed Circuit Board Mounting:

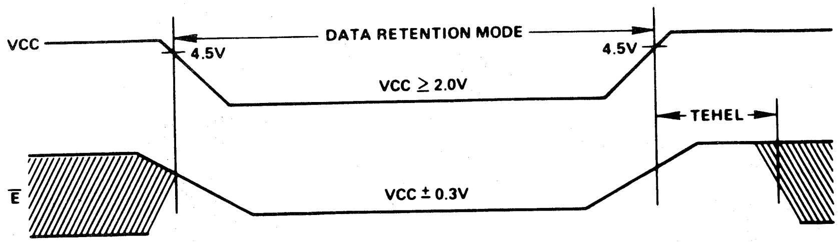
The leadless chip carrier packages used in the HM-6564 have conductive lids. These lids are electrically floating, not connected to VCC or GND. The designer should be aware of the possibility that the carriers on the bottom side could short conductors below if pressed completely down against the surface of the circuit board. The pins on the package are designed with a standoff feature to help prevent the leadless carriers from touching the circuit board surface.

Low Voltage Data Retention

MHS CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC + 0.3V to VCC - 0.3V.
2. On RAMs which have selects or output enables (e.g. $\overline{S}$, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. All other inputs should be held either high (at CMOS VCC) or at ground to minimize ICCDR.
4. Inputs which are to be held high (e.g. $\overline{E}$) must be kept between VCC + 0.3V and 70% of VCC during the power up and power down transitions.
5. The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 volts).

DATA RETENTION TIMING



Board Size Tradeoffs

Printed circuit board real estate is a costly commodity. Actual board costs depend on layout tolerances, density, complexity, number of layers, choice of board material, and other factors.

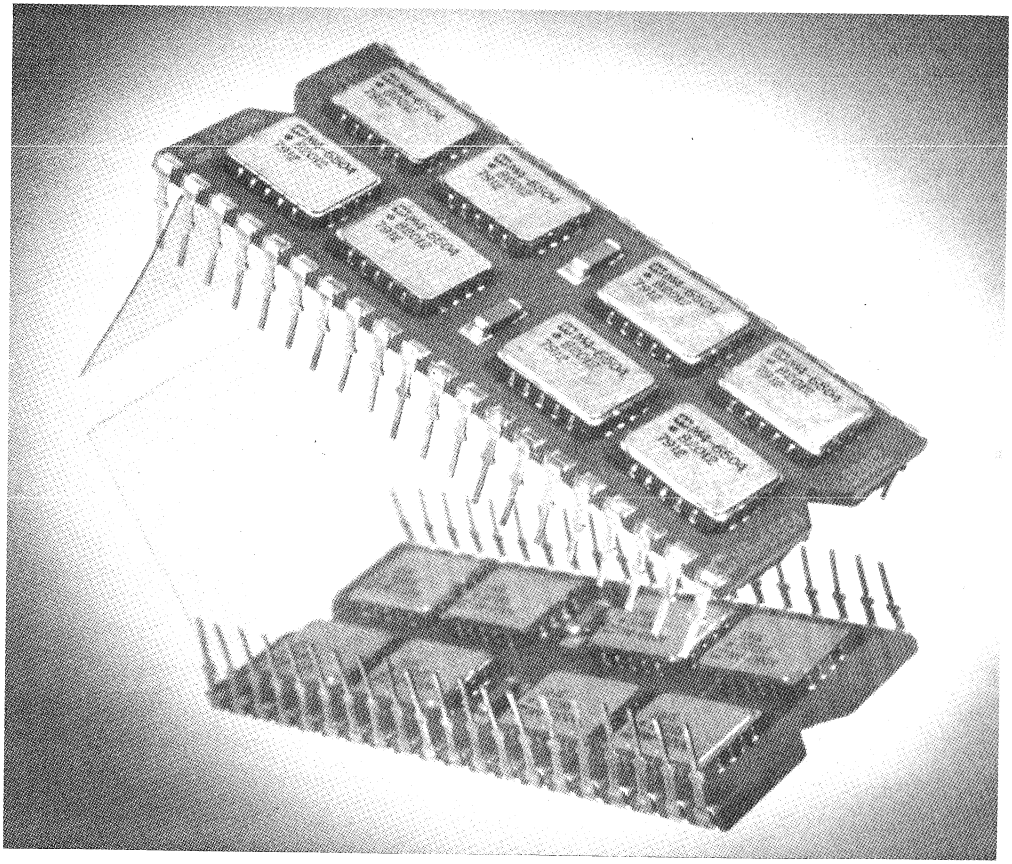
The following table compares board space for 16 standard DIP 4K RAMs to the HM5-6564 RAM array. Both fine line, close tolerance layout and standard "easy" layout board sizes are shown in the comparison.

64K ARRAY OF 16 4K RAMs ON A PC BOARD V.S. THE HM5-6564

PACKAGE	CIRCUIT SUBSTRATE	SIZE
18 Pin DIP	Standard Two Sided PCB	12 to 15 sq. in.
18 Pin DIP	Fine Line or Multilayer PCB	9 to 11 sq. in.
18 Pin Leadless Carrier	Multilayer Alumina Substrate	3 to 5 sq. in.
HM5-6564	Two Sided Mounting Multilayer Alumina Substrate	2 sq. in.

The cost of semiconductor circuits decline with time. If actual costs were included, they would be out of date in a very short time. We urge you to contact your local MHS office or sales representative for accurate pricing allowing cost tradeoff analysis. In your cost analysis, also consider the advantages of a lighter, smaller overall package for your system. Consider how much more valuable your system will be when the memory array size is decreased to about 1/6 of normal size.

2



HM5-6564 – 64K BIT CMOS RAM

ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage - (VCC - GND)	-0.3V to +8.0V	Operating Supply Voltage	+4.5V to +5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Operating Temperature	
		Industrial (-9)	-40°C to +85°C
Storage Temperature	-65°C to +150°C	Military (-2)	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

D.C.

SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current		800	50	μA	IO = 0 VI = VCC or GND
ICCOP1	Operating Supply Current (8K x 8) ②		56	40	mA	f = 1MHz, IO = 0 VI = VCC or GND
ICCOP2	Operating Supply Current (16K x 4) ②		28	20	mA	f = 1MHz, IO = 0 VI = VCC or GND
ICCDR	Data Retention Supply Current		800	25	μA	IO = 0, VCC = 2.0, VI = VCC or GND
VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
IIA	Address Input Leakage	-20	+20	1	μA	GND ≤ VI ≤ VCC
IID1	Data Input Leakage (8K x 8)	-3	+3	.1	μA	GND ≤ VI ≤ VCC
IID2	Data Input Leakage (16K x 4)	-5	+5	.2	μA	GND ≤ VI ≤ VCC
IIE1	Enable Input Leakage (8K x 8)	-10	+10	.5	μA	GND ≤ VI ≤ VCC
IIE2	Enable Input Leakage (16K x 4)	-5	+5	.2	μA	GND ≤ VI ≤ VCC
IIW	Write Enable Input Leakage (Each)	-10	+10	.5	μA	GND ≤ VI ≤ VCC
IOZ1	Output Leakage (8K x 8)	-5	+5	.4	μA	GND ≤ VO ≤ VCC
IOZ2	Output Leakage (16K x 4)	-10	+10	1	μA	GND ≤ VO ≤ VCC
VIL	Input Low Voltage	-0.3	0.8	2.0	V	
VIH	Input High Voltage	VCC-2.0	VCC+0.3	2.0	V	
VOL	Output Low Voltage		0.4	.25	V	IO = 2.0mA
VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
CIA	Address Input Capacitance ③		200	170	pF	f = 1MHz, VI = VCC or GND
CID1	Data Input Capacitance (8K x 8) ③		50	30	pF	f = 1MHz, VI = VCC or GND
CID2	Data Input Capacitance (16K x 4) ③		100	60	pF	f = 1MHz, VI = VCC or GND
CIE1	Enable Input Capacitance (8K x 8) ③		160	100	pF	f = 1MHz, VI = VCC or GND
CIE2	Enable Input Capacitance (16K x 4) ③		80	50	pF	f = 1MHz, VI = VCC or GND
CIW	Write Enable Input Capacitance (Each) ③		100	80	pF	f = 1MHz, VI = VCC or GND
CO1	Output Capacitance (8K x 8) ③		50	30	pF	f = 1MHz, VO = VCC or GND
CO2	Output Capacitance (16K x 4) ③		100	60	pF	f = 1MHz, VO = VCC or GND
CVCC	Decoupling Capacitance	.25		.33	μF	f = 1MHz

NOTES:

① Each individual RAM in the leadless carrier is fully tested at worst case limits of temperature and voltage. The complete assembled HM-6564 array is tested at room temperature only. The worst case parameters are guaranteed over the specified temperature and voltage ranges. Room temperature, 5 volt data is provided for information purposes and is not guaranteed.

② Operating supply current is proportional to operating frequency. ICCOP is specified at an operating frequency of 1MHz, indicating repetive accessing at a 1μs rate. Operation at slower rates will decrease ICCOP proportionally.

③ Capacitance sampled and guaranteed - not 100% tested.

ELECTRICAL CHARACTERISTICS

A.C.

SYMBOL	PARAMETER	TEMP & VCC = OPERATING RANGE MIN	TEMP & VCC = OPERATING RANGE MAX	TEMP = 25°C ① VCC = 5.0V MIN	TEMP = 25°C ① VCC = 5.0V TYP	TEMP = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
TELQV	Chip Enable Access		350		250	300	ns	④
TAVQV	Address Access (TAVQV=TELQV+TAVEL)		400		270	350	ns	④
TELQX	Output Enable	20	120		50	100	ns	④
TEHQZ	Output Disable		120		50	100	ns	④
TELEL	Read or Write Cycle	480		410	320		ns	④
TELEH	Chip Enable Low	350		300	250		ns	④
TEHEL	Chip Enable High	130		110	70		ns	④
TAVEL	Address Setup	50		50	20		ns	④
TELAX	Address Hold	50		50	20		ns	④
TWLWH	Write Enable Low	150		130	100		ns	④
TWLEH	Write Enable Setup	250		220	170		ns	④
TWLEL	Early Write Setup (Write Mode)	10		10	0		ns	④
TWHEL	Write Enable Read Setup	10		10	0		ns	④
TELWX	Early Write Hold (Write Mode)	100		100	70		ns	④
TDVWL	Data Setup	10		10	0		ns	④
TDVEL	Early Write Data Setup	10		10	0		ns	④
TWLDX	Data Hold	100		100	70		ns	④
TELDX	Early Write Data Hold	100		100	70		ns	④
TQVWL	Data Valid to Write (Read-Modify-Write)	0		0	0		ns	④

NOTES:

④ AC Test Conditions:

Inputs - Trise = Tfall ≤ 20ns.
Outputs - CLOAD = 100pF.
Timing measured at 1.5V reference level.

2

ABSOLUTE MAXIMUM RATINGS

Supply Voltage - (VCC - GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage Commercial	+4.5V to +5.5V
Operating Temperature Commercial	0°C to +75°C

ELECTRICAL CHARACTERISTICS

D.C.

SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C VCC = 5.0V ① TYPICAL	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current		4.0	1.0	mA	IO = 0, VI = VCC or GND
ICCOP1	Operating Supply Current (8K x 8) ②		60	45	mA	f = 1MHz, IO = 0 VI = VCC or GND
ICCOP2	Operating Supply Current (16K x 4) ②		30	23	mA	f = 1MHz, IO = 0 VI = VCC or GND
ICCDR	Data Retention Supply Curr.		4.0	0.1	mA	VCC = 2.0, IO = 0 VI = VCC or GND
VCCDR	Data Retention Supply V.	2.0		1.4	V	
IIA	Address Input Leakage	-20	+20	1	μA	GND⩽VI⩽VCC
IID1	Data Input Leakage (8K x 8)	-3	+3	.1	μA	GND⩽VI⩽VCC
IID2	Data Input Leakage (16K x 4)	-5	+5	.2	μA	GND⩽VI⩽VCC
IIE1	Enable Input Leakage (8K x 8)	-10	+10	.5	μA	GND⩽VI⩽VCC
IIE2	Enable Input Leakage (16K x 4)	-5	+5	.2	μA	GND⩽VI⩽VCC
IIW	Write Enable Input Leakage (Each)	-10	+10	.5	μA	GND⩽VI⩽VCC
IOZ1	Output Leakage (8K x 8)	-5	+5	.4	μA	GND⩽VO⩽VCC
IOZ2	Output Leakage (16K x 4)	-10	+10	1	μA	GND⩽VO⩽VCC
VIL	Input Low Voltage	-0.3	0.8	2.0	V	
VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
VOL	Output Low Voltage		0.4	.25	V	IO = 1.6mA
VOH	Output High Voltage	2.4		4.0	V	IO = -0.4mA
CIA	Address Input Capacitance ③		200	170	pF	f = 1MHz, VI = VCC or GND
CID1	Data Input Capacitance (8K x 8) ③		50	30	pF	f = 1MHz, VI = VCC or GND
CID2	Data Input Capacitance (16K x 4) ③		100	60	pF	f = 1MHz, VI = VCC or GND
CIE1	Enable Input Capacitance (8K x 8) ③		160	100	pF	f = 1MHz, VI = VCC or GND
CIE2	Enable Input Capacitance (16K x 4) ③		80	50	pF	f = 1MHz, VI = VCC or GND
CIW	Write Input Capacitance (Each) ③		100	80	pF	f = 1MHz, VI = VCC or GND
CO1	Output Capacitance (8K x 8) ③		50	30	pF	f = 1MHz, VO = VCC or GND
CO2	Output Capacitance (16K x 4) ③		100	60	pF	f = 1MHz, VO = VCC or GND
CVCC	Decoupling Capacitance	.25		.33	μF	f = 1MHz

NOTES:

① Each individual RAM in the leadless carrier is fully tested at worst case limits of temperature and voltage. The complete assembled HM-6564 array is tested at room temperature only. The worst case parameters are guaranteed over the specified temperature and voltage ranges. Room temperature, 5 volt data is provided for information purposes and is not guaranteed.

② Operating supply current is proportional to operating frequency. ICCOP is specified at an operating frequency of 1MHz, indicating repetive accessing at a 1μs rate. Operation at slower rates will decrease ICCOP proportionally.

③ Capacitance sampled and guaranteed - not 100% tested.

2

ELECTRICAL CHARACTERISTICS

A.C.

SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	TEMP. = 25°C VCC = 5.0V ① TYPICAL	UNITS	TEST CONDTIONS
TELQV	Chip Enable Access		450	350	ns	④
TAVQV	Address Access (TAVQV=TELQV+TAVEL)		500	390	ns	④
TELQX	Output Enable	20	150	80	ns	④
TEHQZ	Output Disable		150	80	ns	④
TELEL	Read or Write Cycle	600		450	ns	④
TELEH	Chip Enable Low	450		350	ns	④
TEHEL	Chip Enable High	150		100	ns	④
TAVEL	Address Setup	50		20	ns	④
TELAX	Address Hold	50		20	ns	④
TWLWH	Write Enable Low	150		100	ns	④
TWLEH	Write Enable Setup	250		170	ns	④
TWLEL	Early Write Setup (Write Mode)	10		0	ns	④
TWHEL	Write Enable Read Setup	10		0	ns	④
TELWX	Early Write Hold (Write Mode)	100		70	ns	④
TDVWL	Data Setup	10		0	ns	④
TDVEL	Early Write Data Setup	10		0	ns	④
TWLDX	Data Hold	100		70	ns	④
TELDX	Early Write Data Hold	100		70	ns	④
TQVWL	Data Valid to Write (Ready-Modify-Write)	0		0	ns	④

NOTES:

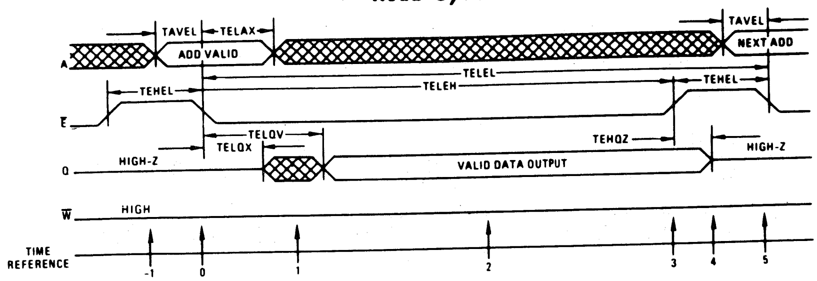
④ AC Test Conditions:

Inputs – Trise = Tfall ≤ 20ns.

Outputs – CLOAD = 100pF.

Timing measured at 1.5V reference level.

Read Cycle

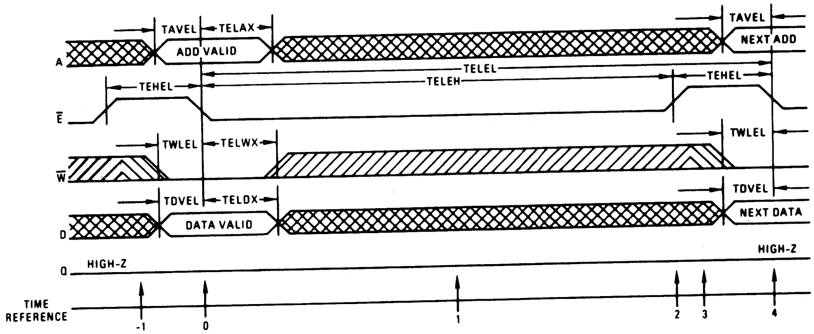


TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	OUTPUT Q	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	OUTPUT ENABLED
2	L	H	X	V	OUTPUT VALID
3	↗	H	X	V	READ ACCOMPLISHED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set up and hold time requirements must be met. After the requir-ed hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until during time (T = 2). $\overline{W}$ must remain high until after time (T = 2). After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the output buffer and ready the RAM for the next memory cycle (T = 4).

Early Write Cycle



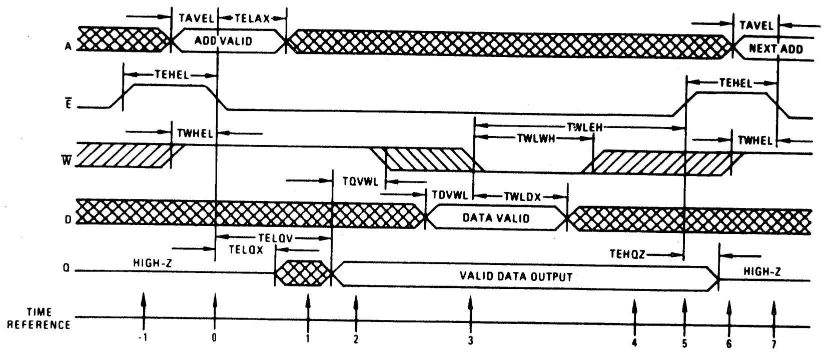
TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	L	V	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	X	X	X	Z	WRITE IN PROGRESS INTERNALLY
2	↗	X	X	X	Z	WRITE COMPLETED
3	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS 1)
4	↘	L	V	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The early write cycle is the only cycle where the output is guaranteed not to become active. On the falling edge of $\overline{E}$ (T = 0), the addresses, the write signal, and the data input are latched in on chip registers. The logic value of $\overline{W}$ at the time $\overline{E}$ falls determines the state of the output buffer for that cycle. Since $\overline{W}$ is low when $\overline{E}$ falls, the out-put buffer is latched into the high impedance state and will remain in that state until $\overline{E}$ returns high (T = 2). For this cycle, the data input is latched by $\overline{E}$ going low; there-fore data set up and hold times should be referenced to $\overline{E}$. When $\overline{E}$ (T = 2) returns to the high state the output buffer disables and all signals are unlatched. The device is now ready for the next cycle.

2

Read Modify Write Cycle

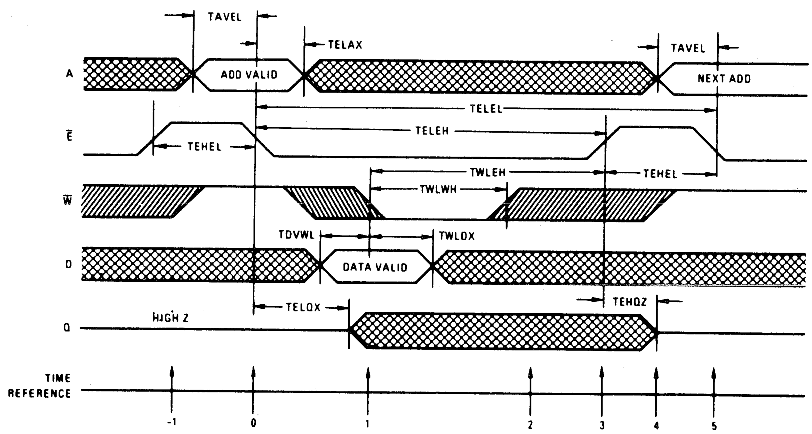


TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↓	H	V	X	Z	CYCLE BEGINS, ADDRESS ARE LATCHED
1	L	H	X	X	X	OUTPUT ENABLED
2	L	H	X	X	V	OUTPUT VALID, READ AND MODIFY TIME
3	L	↓	X	V	V	WRITE BEGINS, DATA IS LATCHED
4	L	X	X	X	V	WRITE IN PROGRESS INTERNALLY
5	↑	X	X	X	V	WRITE COMPLETED
6	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
7	↓	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The read modify write cycle begins as all other cycles on the falling edge of $\overline{E}$ (T= 0). The $\overline{W}$ line should be high at (T = 0) in order to latch the output buffers in the active state. During (T = 1) the output will be active but not valid until (T = 2). On the falling edge of the $\overline{W}$ (T = 3) the data present at the output and input are latched. The $\overline{W}$ signal also latches itself on its low going edge. All input signals excluding $\overline{E}$ have been latched and have no further effect on the RAM. The rising edge of $\overline{E}$ (T = 5) completes the write portion of the cycle and unlatches all inputs and the output. The output goes to a high impedance and the RAM is ready for the next cycle.

Late Write Cycle



TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	⌄	H	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	⌄	X	V	X	WRITE BEGINS, DATA IS LATCHED
2	L	H	X	X	X	WRITE IN PROGRESS INTERNALLY
3	⌃	H	X	X	X	WRITE COMPLETED
4	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	⌄	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

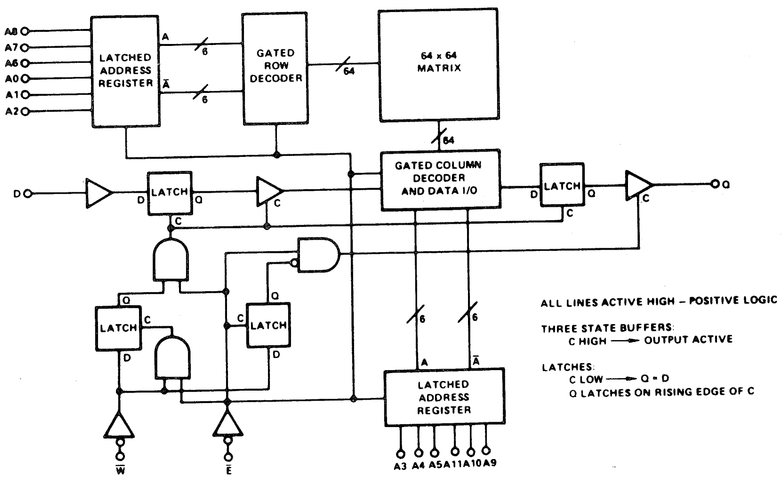
The late write cycle is a cross between the early write cycle and the read-modify-write cycle.

Recall that in the early write the output is guaranteed to remain high impedance, and in the read-modify-write the output is guaranteed valid at access time. The late write is between these two cases. With this cycle the output may become active, and may become valid data, or may remain active but undefined. Valid data is written into the RAM if data set up, data hold, write setup and write pulse widths are observed.

NOTES:

In the above descriptions the numbers in parenthesis (T = n) refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

HM-6504 (One of Sixteen)



MATRA-HARRIS SEMICONDUCTEURS

data sheet

HM 65681
4K × 4
CMOS STATIC RA

ADVANCE INFORMATION

2

Features

.ASYNCHRONOUS
.FAST ACCESS TIME : 70 ns max
.STAND BY CURRENT : 50 μA Max
.OPERATING SUPPLY CURRENT : 10 mA Max (1 MHz)
.DATA RETENTION : 2 V MM@50 μA
.STATIC OPERATION : NO CLOCK OR REFRESH REQUIRED
.INDUSTRY STANDARD PIN OUT
.GATED INPUT BUFFER
.WIDE TEMPERATURE RANGE SPEC'S − 55° C TO + 125° C
.SINGLE SUPPLY : 5 V

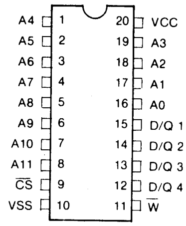
Description

.The HM 65681 is a 16384 bits static Random access memory organized as a 4K words by 4 bits using CMOS technology and operates from the 5 V supply.

.The HM 65681 uses "state of the art" MHS technology, the scaled self aligned junction isolation featuring low stand by current and fast address access time.

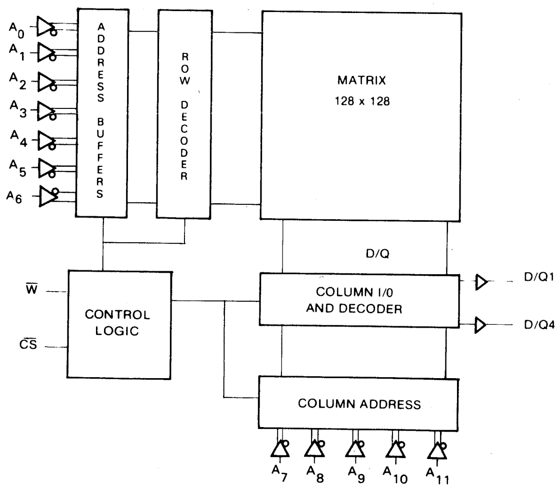
.The HM 65681 features fully static operating requiring no external clocks or timing strobes, equal access and cycle times. A judicious choice has been made decreasing consumption and optimising the speed. The device utilizes and edge activated circuit design for asynchronous operation and fast cycle time.
The pin out in the JEDEC 20 pin 300'' width package allowing maximum board packing density.

Pinout

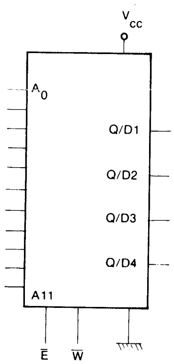


TOP VIEW

A : Address input
D/Q : Data in/out
$\overline{CS}$: Chip select
$\overline{W}$: Write enable



Logic Symbol



MATRA-HARRIS SEMICONDUCTEURS

data sheet

HM 6816A
2K × 8
CMOS EEPROM

ADVANCE INFORMATION

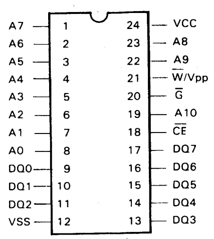
Features

- SINGLE SUPPLY : 5 V only
- COMPATIBLE WITH PRIOR EEPROM'S GENERATIONS
- CHIP AND BYTE ERASE : 10 ms
- FAST ACCESS : 200 ns max
- LOW STAND BY CURRENT : 100 µA max
- LOW OPERATING CURRENT : 10 mA max @1 MHz
- ASYNCHRONOUS
- GATED INPUTS
- INDUSTRY STANDARD PIN OUT
- TTL INPUT COMPATIBLE FOR READ AND WRITE OPERATION
- "THREE STATE" OUTPUT CONTROL WITH $\overline{G}$ AND $\overline{CE}$
- 10 000 ERASE/WRITE CYCLES

Description

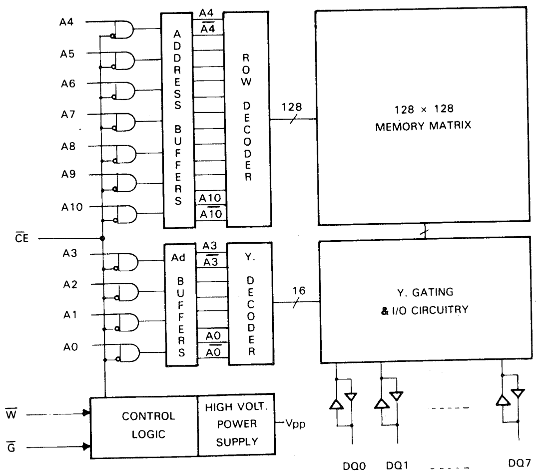
- The HM 6816 is a 16384 bits Electrical Erasable Programmable Read only Memory organized as 2048 words by 8 bits, using CMOS technology and operates from the single 5 V supply.
- The HM 6816 uses "state of the art" MHS technology. The scaled self aligned junction isolation featuring low current and fast address access time.

Pinout



A : Address input
DQ : data input/output
$\overline{CE}$: Chip Enable
$\overline{G}$: Output Enable
$\overline{W}$/Vpp : Read/Program or Erase

Functional Diagram



Functional Table

MODE	$\overline{CE}$	$\overline{G}$	$\overline{WE}$	I/O
• Read	L	L	H	Data out
• Stand by	H	X	X	Z
• Output disable	L	H	X	Z
• Byte erase	L	H	L/Vpp	Din = VIH
• Byte program	L	H	L/Vpp	Data in
• Program inhibition	H	X	X	Z
• Chip erase	L	Vpp	L/Vpp	Z
Features added to improved testability				
Bloc write	Vpp	Vpp	L/Vpp	Data in*
Erase margin	Vpp	Vpp	L/Vpp	Din = H**
Read margin	L	L	L	Data out***

* During this operation the information presented on the I/O pins if loaded into half of the memory according to Xo/$\overline{Xo}$ pin A10.

** Bloc erase operation on half of the memory according to Xo/$\overline{Xo}$.

*** Read operation with harder condition to test programmed states only.

2

CMOS gate arrays 3

3

MHS MATRA-HARRIS SEMICONDUCTEURS

data sheet

MA 0250-MA 0400-MA 0800-MA 1200

HIGH SPEED CMOS GATE ARRAYS

Features

- HIGH SPEED CMOS : 2 NS/GATE TYPICAL PROPAGATION DELAY.
- LOW CONSUMPTION :
  - STAND BY CURRENT 10 nA/GATE
  - OPERATING CURRENT 5 μA/GATE/MHz
- 250 TO 1200 2-INPUT GATE COMPLEXITY.
- 8 TO 68 PIN PACKAGES (PLASTIC DIL, CERDIP, LCC).
- POWER SUPPLY RANGE : 3 TO 7 V.
- WIDE TEMPERATURE RANGE : – 55° C TO + 125° C.
- COMPLETE INPUT/OUTPUT FLEXIBILITY.
- TTL/CMOS INPUT COMPATIBILITY.
- TTL OUTPUT COMPATIBILITY : 2 TTL LOADS (OR 10 TTL/LS LOADS).
- INPUT PROTECTION NETWORK.
- EXTENSIVE LS OR HCMOS SSI/MSI FUNCTIONS LIBRARY.
- COMPLETE CAD SOFTWARE PACKAGE.

Description

The MA 0250-MA 0400-MA 0800-MA 1200 Gate Array product family from Matra-Harris Semiconducteurs is using "state of the art" advanced silicon gate CMOS technology. This process, called Scaled SAJI IV, features drawn channel lengths of maximum 2.5 μ and 3 μ respectively for N and P channels.

Designed for digital applications, the Matra-Harris array structure presents an internal predefined matrix organized in rows of uncommitted basic cells and interconnect routing channels, the matrix being surrounded by flexible input/output cells.

These gate arrays are used to implement combinatorial and sequential logic functions (registered in the MHS cell library) on the same chip and connect them with a unique metal layer corresponding to the user's own specific requirements.

The use of MHS CAD softwares permits users to achieve this goal within a fast and reliable design cycle time.

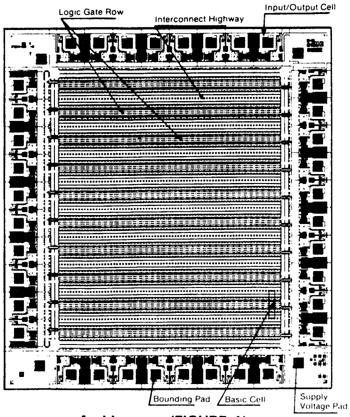
3

MA 0250-MA 0400-MA 0800-MA 1200 FAMILY :

PART NUMBER	GATE COUNT	I/O PADS	INPUT/POWER PADS	TOTAL PADS	METAL LEVEL	PACKAGE OPTIONS PIN	N CHANNEL LENGTH
MA-0250	228	28	4	32	1	8 to 40	2.5 μ
MA-0400	380	36	4	40	1	8 to 40	2.5 μ
MA-0800	754	50	4	54	1	22 to 64	2.5 μ
MA-1200	1139	62	4	66	1	24 to 68	2.5 μ

NOTE : 1 gate is the equivalent of a 2 input NAND or NOR gate (It means 2 N and 2 P channel transistors).

GATE ARRAY PRODUCT DESCRIPTION :



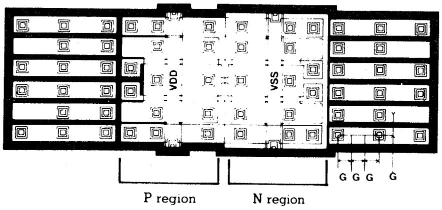
Architecture (FIGURE 1)

ARCHITECTURE

The MHS gate array structure presents as an internal matrix of uncommitted logic gates organized in rows. Each row is separated from the other by an interconnect highway area where metal channels are routed.

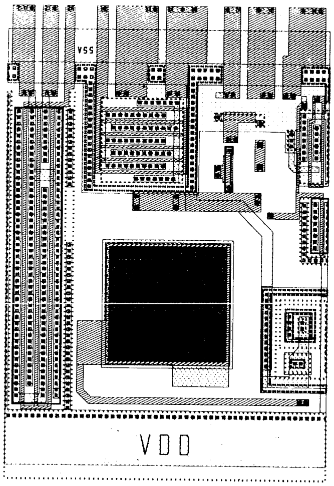
The matrix is surrounded by peripheral cells allowing the gate array to interface with external circuitry.

BASIC CELL



The basic cell (gate) consists of 2 pairs of N and P channels MOS transistors associated with 2 feed-thru in low resistivity polysilicon. An all metal supply distribution is achieved within the cell by 2 wide Aluminium lines able to support strong current surges that may be required at high frequency operation of a circuit. One contact per cell between these supply lines and the substrate and the P-well achieves a regular bias all through the matrix.

PERIPHERAL CELL



Peripheral cell (FIGURE 3)

The peripheral cell confirms the versatility of MHS array by providing an additional and total flexibility on input/output configurations.

The peripheral cell can be customized as :

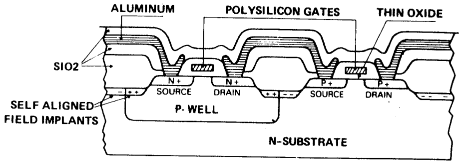
- TTL input
- CMOS input
- Direct input (for Schmitt trigger input)
- Output buffer :
  All outputs are capable of driving 2 TTL or 10 LS TTL loads. Additional drive capability may be obtained by connecting output buffers in parallel (up to 20 LS TTL loads).
- Open Drain Output
- Tri-State Output
- Bidirectional input/output
- VDD or VSS Supply

Furthermore, the peripheral cell contains :

- 2 High impedance transistors which can be used as pull-up or pull-down (140 K ohm typically)
- an input protection network against parasitic phenomenons such as electrostatic damage and latch up triggering

PROCESS DESCRIPTION :

MHS High Speed CMOS Gate Arrays are constructed using the self-aligned junction isolated (Scaled SAJI IV) process with a cross section shown in Fig. 4.



CMOS scaled SAJI IV process cross section (FIGURE 4)

The association of a 3 microns lithography and a self aligned CMOS processing provides electrical parameters which permit the realization of fast digital circuits.

By using local oxidation to separate adjacent active regions, a high packing density of chips is achieved together with a lowering of field and side wall capacitances. Self aligned field implants are utilized to increase the field transistor threshold and to lower the N- substrate and P- well resistance which contribute to latch up behavior improvement. Some key figures of the scaled SAJI IV process are listed in Fig. 5.

PARAMETERS	VALUE
THIN OXIDE THICKNESS	450Å
DRAWN TRANSISTOR LENGH	
P CHANNEL TRANSISTOR	3μM
N CHANNEL TRANSISTOR	2.5μM
TRANSISTOR THRESHOLD	
VTN	0.75 VOLTS
VTP	0.75 VOLTS

PARAMETERS	VALUE
FIELD TRANSISTORS THRESHOLD	>15 VOLTS
METAL PITCH	10μM
SUBSTRATE	N– <100>
DOPING AGENT N	ARSENIC
P	BORON

Some key figures of the scaled SAJI IV process (FIGURE 5)

MHS, SSI/MSI CELL LIBRARY :

The MA- series of arrays is supported by a complete and extended library of precharacterized and predefined SSI/MSI logic functions. The user will find in this cell library equivalent logic functions to 74 LS or 74 HC SSI/MSI standard products.

In this library any cell has its own data sheet including logic specification and diagram topological characteristics, electrical data and logic simulator reference as it can be seen on Fig. 6.

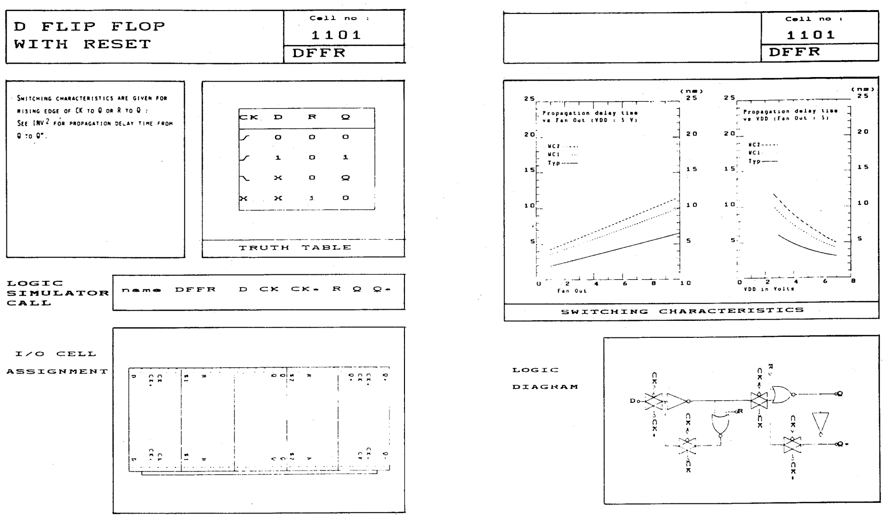
The propagation delay of each cell is given as a function of 3 parameters which are Fan Out of the cell, operating temperature, and power supply. Typical and worst cases values are given.

The library of internal cells provides more than 80 SSI/MSI logic functions like :

- Combinatorial logic functions
- Sequential logic functions
- MSI complex functions.

The peripheral cell library offers a wide range of interfacing external circuitry to the array :
- TTL or CMOS compatible input
- Output buffers (tri-state, open drain...)
- Bidirectionnal input/output
- Oscillator buffers (interfacing with external oscillator...).

A complete list of MHS cell library is given on Fig. 7.



Data sheet of library cell (D Flip Flop) (FIGURE 6)

MHS MACROCELL LIBRARY DESCRIPTION : (FIGURE 7)

MACROCELL	GATE EQUIVALENT
Combinatorial logic functions	
- 2 input NAND	1
- 3 input NAND	2
- 3 input NAND + 1 Inverter	2
- 4 input NAND	2
- 5 input NAND	3
- 8 input NAND	6
- 2 input NOR	1
- 3 input NOR	2
- 3 input NOR + 1 Inverter	2
- 4 input NOR	2
- 5 input NOR	4
- 8 input NOR	6
- 2 input AND	2
- 2 input AND + 1 Inverter	2
- 3 input AND	2
- 4 input AND	3
- 4 input AND + 1 Inverter	3
- 2 input OR	2
- 2 input OR + 1 Inverter	2
- 3 input OR	2
- 4 input OR	3
- 4 input OR + 1 Inverter	3
- 2 input Exclusive OR	3
- 2 input Exclusive NOR	3
- Inverter	1
- Dual Inverter	1
- Serial Inverters	1
- Power Inverter	1
- 2 input AND into 2 input OR-Invert	2
- Dual 2 input AND's into 2 input OR-Invert	3
- Dual 3 input AND's into 2 input OR-Invert	3
- Dual 4 input AND's into 2 input OR-Invert	4
- 2 input OR/AND into 2 input OR-Invert	2
- Dual 2 input OR's into 2 input AND-Invert	2

MACROCELL	GATE EQUIVALENT
- Dual 3 input OR's into 2 input AND-Invert	3
- 2 input OR into 2 input AND into 2 input OR-Invert	2
- 2 input OR/3 input OR/4 input OR into 4 input AND-Invert	5
- 2 input AND into 2 input OR/ 2 input OR into 2 input AND-Invert	3
- *1 bit full adder with carry	7
- *1 bit full adder with fast carry path	9
- *1 bit simple adder	4
Sequential Logic Functions	
- Latch	2
- Latch with R (reset)	3
- Latch with S (set)	3
- Latch with $\overline{R}$	3
- Latch with $\overline{S}$	3
- D Flip Flop	4
- D Flip Flop with R (reset)	5
- D Flip Flop with S (set)	5
- D Flip Flop with $\overline{R}$	5
- D Flip Flop with $\overline{S}$	5
- D Flip Flop with R and S	6
- D Flip Flop with $\overline{R}$ and $\overline{S}$	6
- D Flip Flop with 1 clock	5
- JK Flip Flop	7
- JK Flip Flop with R (reset)	8
- JK Flip Flop with S (set)	8
- JK Flip Flop with $\overline{R}$	8
- JK Flip Flop with $\overline{S}$	8
- JK Flip Flop with S and R	9
- JK Flip Flop with $\overline{S}$ and $\overline{R}$	9
- RS Flip Flop with NAND	2
- RS Flip Flop with NOR	2

MACROCELL	GATE EQUIVALENT
Sequential Logic Functions (cont'd)	
- Toggle Flip Flop with asynchronous parallel load	12
Interface and Special Functions	
- *TTL compatible Schmitt Trigger	6
- CMOS compatible Schmitt Trigger	2
- Enable command for 3 state Output Buffer	5
- *Retriggerable resetable Monostable (with external RC)	10
- Transfer Gate	1
- Bidirectional 2-1 (de) multiplexer	1
- Inverting 3 state internal bus driver	2
- Non-inverting 3 state internal bus driver	3

MACROCELL	GATE EQUIVALENT
MSI functions	
- 4 bit full adder (4008)	68
- 4 bit static shift register (4015) (serial input/parallel output)	24
- 4 bit static shift register (4035) (parallel input/parallel output)	46
- 14 bit binary counter (4020)	75
- Decode counter/divider (4017) (+ 10 decoded decimal outputs)	54
- 4 bit binary counter (4163) (with synchronous clear)	56
- Binary up/down counter (4516)	76
- Binary up counter (4520)	30
- Binary to 1-of-4 decoder (4556)(Inverting)	8
- 4 bit magnitude comparator (4585)	30

MHS CAD SOFTWARE SUPPORT :

MHS developed a complete CAD Software package in order to insure a fast and efficient gate array development with minimal risks.

MHS CAD Softwares provide :

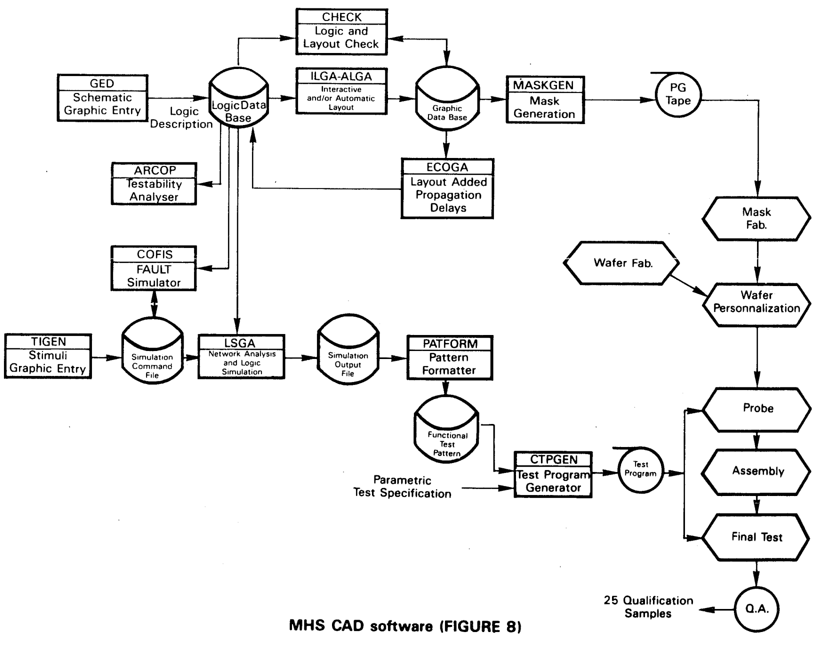
- A way for a system, rather than a circuit, designer to integrate his logic circuit into silicon
- A full continuity between the different design steps from logic architecture description to chip testing
- A circuit development without breadboard realization, thanks to a logic simulation using realistic propagation delays. It has been made possible by a precise, but user's transparent, modelization of the device and network behaviour
- Documentation aids (schematic, simulation results, symbolic lay out, mask plots).

MHS CAD Softwares use 2 common data bases :

- A logic data base containing the complete description of customer circuit. Used as reference file. Most of the programs access this data base allowing to issue a logic simulation fitting with the physical reality and to generate a test program
- A Graphic Data Base containing the lay-out in symbolic form is generated by interactive and/or automatic placement and routing program. Software use this file to make correspondences :
  - from Graphic symbolic to logic
  - from Graphic symbolic to mask

MHS CAD SOFTWARE SUPPORT :

MHS available software are presented in Fig. 8.



MHS CAD software (FIGURE 8)

Above development flow shows very clearly the different steps in a gate array design. Two parallel ways with interactive links are taken in order to achieve a full gate array design : Lay-out and Test. The finalization of such a design is the issue of :

- a PG tape for mask tooling
- a Test Program magnetic tape for probe and Final Test of the silicon.

The heart of this Gate Array development flow is the logic data base.

MHS CAD SOFTWARE SUPPORT :

GED : Graphic Editor :
Provides a graphic entry of logic schematic. Outputs are a connection list and plots for production documents.

LSGA : Logic Simulator for Gate Arrays :
In addition to normal possibilities of a modern interactive or batch mode logic simulator working with 9 logic states (i.e, timing control and spikes detection) it offers some extra features :

- a unit delay (pseudo functional) simulation mode
- a network analyser and operating conditions scaler calculating separate rise and fall propagation delay times
- a test option verifying toggle; it assures that all nodes in the network have been exercised
- a logic analyser output (WAVE) permitting to analyse the functionality of the circuit and by changing the sampling period to check propagation delay times
- a compatibility with TEGAS* and LOGIS* simulators.

ARCOP : Testability Evaluation Program :
It's a controllability/observability program, allowing users to improve testability of the circuit.

COFIS : Fault Simulator :
Is a concurrent Fault simulator using tables generated from the logic description to perform a single stuck-at fault generation and fault analysis and produce a full detection report.

ILGA : Interactive Placement and Routing :
Is a graphic editor providing easy way to place and move the cells, to route metal interconnect channels. Routing task is facilitated because special symbols indicate I/O in the current connection. Partial or total symbolic plots of the circuit can be drawn for documentation use.

CHECK : Lay-Out and Design Rule Checker :
Is ILGA's complement. It checks correspondence between logic description and lay-out and detects design rules violations. Intermediate checking capabilities limits the risk of serious mistakes and ensures a good final lay-out.

ALGA : Automatic Placement and Routing :
Automatic Placement and Routing in 1 level of interconnect is automatically performed. ILGA is therefore useful to preplace cells (pads for instance), to check the lay-out and to route some possible unrouted connections. 80 % silicon use is normally expected with fully automatic routing.

ECOGA : Electric Checking of Gate Arrays :
For each equipotential line the total length of metal and polysilicon is computed. It gives worst case capacitance and resistance values and therefore additional parasitic delays. A new simulation taking into account delays over standard value can now be run.

PATFORM : Test Pattern Formatter :
Logic simulation output file is the basis of functional testing which is made on Sentry test equipment. PATFORM is an intelligent translater generating and compacting bit patterns and inserting logical mask to prevent erroneous sampling.

CTPGEN : Conversational Test Program Generator :
Is an editor permitting easy construction of test program by assembling the functional subtest generated by PATFORM to other modules for DC and AC standard parametric test measurements.

All these programs are running on VAX 11/780 DEC computer using Tektronix Graphic Terminals (40XX and 41XX series).

They are also running on Matra Design Systems stand-alone work station ("Gate Mark")*.

HAL SUPPORT :

As 74LS/7400/4000/74HC series SSI/MSI functions can be implemented on MHS gate array chip, it is possible to convert PAL/FPLA design to gate arrays.

The MA0250 is well suited for these HAL (Hard Array Logic) applications : the HAL is for PAL, what the ROM is for PROM.

A special software will perform the direct translation from boolean expression to logic data base and then to final HAL product.

** Trademarks : LOGIS is a trademark of Information Systems Design incorporated*
TEGAS is a trademark of Comsat General Integrated Systems.

"Gate Mark" is a trademark of Matra Design Systems .

PAL is a trademark of Monolithic Memories incorporated.

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MHS/CUSTOMER INTERFACE : MHS DESIGN APPROACHES :

In order to give customer an easy access to CAD facilities, MHS offers a broad range of Design approach solutions. Each approach offered by MHS is well suited to customer needs according to customer CAD design resources, CAD design know how, CAD equipment facilities.

MHS proposes :

1) for customers willing to design their circuit themselves.
   - remote mode access to Nantes CAD center via modem phone line (1200/2400 BPS) and/or specialized data transmission network (9600 BPS).
   - local mode capabilities by transfering to customer, having its own CAD center, the graphic data base and softwares
   - local mode design by using the ''Gate Mark'' stand alone work station
   - MHS Regional Design Centers where customer will find equipment and technical support.

2) For customers willing to sub-contract the design of their circuit
   - MHS local design resources capabilities in Nantes CAD Center and Regional Design Centers
   - Independant CAD-Test Design Houses qualified by MHS and supported by MHS engineering.

The Fig. 9 summarizes the MHS Design Approaches

DESIGN APPROACHES	OPTIONS	AVAILABILITY DATE	EQUIPMENT NEEDED AT CTM LOCATION	DEVELOPMENT CHARGES
Design done by customer on remote mode - Modem phone line (1200-2400 BPS) - Data transmission network (4800-9600 BPS)	At customer location	Available	• TEKTRONIX graphic terminal • Modem	• Training course • CAD development • Test
	At MHS plant (direct access) - 4113 A/4014/4114 graphic terminal - Work station	Available	None	• Training course • CAD development • Test • Tektronix rental
	At MHS regional office - 4113 A graphic terminal - Work station	Q4 - 83	None	• Training course • CAD development • Test • Telephone line rental • Tektronix rental
Design done by customer on local mode	By using Matra Design Systems work station	Q4 - 83	• Stand alone work station ''Gate Mark''	• Training course • Handling + mask charges • Test
	By using his own CAD softwares	Available	• Computer • Graphic system (calma preferable)	• Gate array matrix + cell library transfer • Handling + mask charges
	By using MHS CAD softwares	Q4 - 83	• VAX 11 computer • Tektronix graphic terminal	• Training course • Gate array matrix + cell library transfer • CAD software transfer • Handling + mask charges • Test
Design done by	MHS	Available	None	• CAD development • Engineering charges • Test
	MHS representative Design-Test House	Available	None	• Representative charges

MHS Gate Array Design Approaches (FIGURE 9)

HIGH SPEED CMOS GATE ARRAY CHARACTERISTICS :

ABSOLUTE MAXIMUM RATINGS :

PARAMETER	SYMBOL	LIMITS	UNIT
DC Supply Voltage	VDD	−0.5 to +7	Volt
Input/Output Voltage	V_{IN}/V_{OUT}	−0.3 to VDD + 0.3	Volt
Storage Temperature	T_{stg}	−65 to +150	° C

RECOMMENDED OPERATING CONDITIONS :

PARAMETER	SYMBOL	LIMITS	UNIT
DC Supply Voltage	VDD	3 to 6	Volt
Input/Output Voltage	V_{IN}/V_{OUT}	0 to VDD	Volt
High or Low level output current	I_{OUT}	0 to − 5 / + 15	mA
Operating Temperature Range	Military (−2) Industrial (−9) Commercial (−5)	−55 to +125 −40 to + 85 0 to + 70	° C

DC ELECTRICAL CHARACTERISTICS :

(Specified at VDD = 5 V ± 10 % and all temperature ranges unless otherwise notified)

PARAMETER	MIN	TYP*	MAX	UNIT	CONDITIONS
Low Level Input Voltage VIL CMOS (BUFIN MOS) VIL TTL (BUFIN TTL)			1.5 0.8	V V	VOUT = 4.5 V IOUT = 0
High Level Input Voltage VIH CMOS (BUFIN MOS) VIH TTL (BUFIN TTL)	3.5 2 2.2			V V V	VOUT = 0.5 V IOUT = 0 (0/+ 70° C) (− 40/+85° C)(− 55/+125° C)
Low Level Output Voltage VOL (BUFOUT)			0.4	V	VIN = VDD IOL = − 3.2 mA
High Level Output Voltage VOH (BUFOUT)	3.9			V	VIN = 0 V IOH = 100 μA
High Level Output Voltage VOH (BUFOUT)	2.4			V	VIN = 0 V IOH = 5 mA
Input Leakage Current IIL, IIH (without pull-up)	− 1 − 3 − 5		+ 1 + 3 + 5	μA	VIN = VDD or 0 V 0° C to + 70° C − 40° C to + 85° C − 55° C to + 125° C
3 State Output Leakage current IOZ	− 1 − 3 − 5		+ 1 + 3 + 5	μA	VIN = VDD or 0 V 0° C to + 70° C − 40° C to + 85° C − 55° C to + 125° C
Standby Current IDDSB		10		nA/gate	VIN = VDD or VSS
Operating Current IDDOP		5		μA/gate /MHz	VIN = VDD or VSS

* *Typical values are given at VDD = 5V, TA = 25° C.*

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AC ELECTRICAL CHARACTERISTICS :

(Specified at VDD = + 5 V)

PARAMETER		0° C to + 70° C		– 40° C to + 85° C		– 55° C to + 125° C		UNIT
		TYP	MAX	TYP	MAX	TYP	MAX	
Inverter Propagation Delay tp	(1)(2)	1.3	3	1.5	3.5	1.7	4	ns
2 input NAND Prop. Delay tp (NAND2)	(1)(2)	1.8	4	2	4.5	2.3	5	ns
2 input NOR Prop. Delay tp (NOR2)	(1)(2)	2.1	5.5	2.4	6	2.7	7	ns
4 input NAND Prop. Delay tp (NAND2)	(1)(2)	1.9	4.5	2.2	5	2.4	6	ns
4 input NOR Prop. Delay tp (NOR4)	(1)(2)	4	10	4.6	10.5	5.2	11	ns
D Flip Flop with R Prop. Delay tp (DFFR*)	(1)(2)(3)	4	12	4.5	13.5	5	16	ns
CMOS compatible input buffer Prop. Delay tp (BUFIN MOS)	(1)(2)	2.2	7	2.7	7.5	3	9	ns
TTL compatible input buffer Prop. Delay tp (BUFIN TTL)	(1)(2)	2.2	7	2.7	7.5	3	9	ns
Output Buffer Prop. Delay tp (BUFOUT)	(1)(4)	13	20	14	22	15	25	ns
Output Buffer Rise Time (10 % - 90 %) tr (BUFOUT)	(4)	18	25	20	27	25	32	ns
Output Buffer Fall Time (90 % - 10 %) tf (BUFOUT)	(4)	15	20	17	22.5	20	28	ns

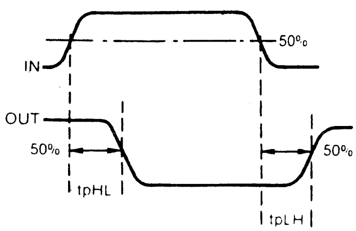
AC TEST CONDITIONS :

(1) All propagation delay times are average values between input signal and output signal.

Propagation delay values given in this table are average values between tpLH and tpHL.

$$tp = \frac{tpLH + tpHL}{2}$$

Signal levels are
VIL = 0 Volt
VIH = VDD



(2) Propagation delays of internal cells and input buffers are given under following conditions :
Fan out = 2 + 500 um metal interconnect + 480 um of polysilicon

(3) D Flip Flop (with R) propagation delay is corresponding to propagation delay between clock (CK) and output (Q)

(4) BUFOUT cell test conditions are :
Load Capacitance CL = 50 pF

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PACKAGING :

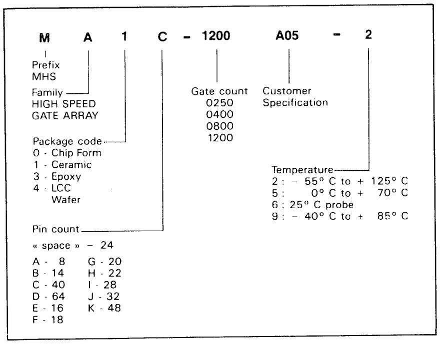
MHS High speed CMOS gate arrays package options

PACKAGE TYPE	LEAD COUNT	MA 0250 MA 0400	MA 0800	MA 1200
Plastic DIL	8	×		
	14	×		
	16	×		
	18	×		
	20	×		
	22	×	×	
	24	×	×	×
	28	×	×	×
	40	×	×	×
Ceramic DIL	16	×		
	18	×		
	20	×		
	22	×	×	
	24	×	×	×
	28	×	×	×
	40	×	×	×
	48 (side brazed)		×	×
	64 (side brazed)			×
LCC	28	×		
	32	×	×	
	40	×	×	×
	48		×	×
	64		×	×

A wide variety of packages is offered for the 1 metal layer MHS gate array product family. Other packages may be available on customer request after MHS approval.

MHS can also deliver gate array products in dice or wafer form.

PRODUCT DEFINITION :



HIGH SPEED CMOS EVALUATION TEST VEHICLE :

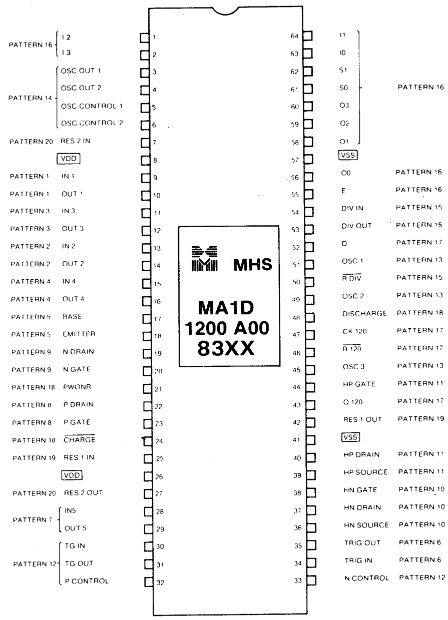
The MA1D-1200A00 is the test vehicle of the 1 metal layer MHS array family. It has been specifically patterned in order to evaluate AC and DC characteristics of these products.

The main patterns implemented on this chip are :

- Input/Output Buffers
- Transfer Gate
- Ring Oscillator
- Frequency Divider by 8
- 4 bit Shifter
- 120 Bit Static Shift Register
- Power on Reset

This test vehicle is available in small sample quantities.

A data log is delivered with the samples.



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GATE CENTERS

FRANCE

- Nantes Centre Électronique
  La Chantrerie
  44075 - B.P. 942
  Tél. (40) 49.08.20
  Twx : 711 930 F

GERMANY

- Munich Harris MHS
  Erfurterstrasse 29
  8057 Eching
  Tel : 089-3191035
  Twx : 5213866

FUTURE EXTENSION

U.K. HARRIS-MHS Slough
ITALY HARRIS-MHS Milan
FRANCE MHS Le Chesnay

GATE HOUSES

FRANCE/SPAIN

- Toulouse Systèmes Sud
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  Z.I. Est
  31770 Colomiers
  Tél. : (61) 78.81.52
  Twx : 530 014 F

GERMANY

- Munich Mikron
  Oscar-Von-Miller-Strabe 1A
  8057 Eching bei München
  Tel : 08165/77240
  Twx : 526722 Mikro

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- California Matra Design Systéms
  2840-100 San Thomas
  Express Way
  Santa Clara
  CA-95051
  Tél. : 408/986.9000

FUTURE EXTENSION

SCANDINAVIA

CMOS microprocessor 4

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Product Index

ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under ''Absolute Maximum Ratings'' may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect devices reliability. The conditions listed under ''Electrical Characteristics'' are the only conditions recommended for satisfactory operation.

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MHS
MATRA-HARRIS SEMICONDUCTEURS

data sheet

80C48 - 80C35
CMOS SINGLE-COMPONENT 8-BIT MICROCOMPUTER

PRELIMINARY

80C48 Low Power Mask Programmable ROM
80C35 Low Power, CPU Only

- PIN-TO-PIN COMPATIBLE WITH MHS' 8048H/8035HL
- 2.5 µ SEC. INSTRUCTION CYCLE AT 6 MHz CLOCK ALL INSTRUCTIONS 1 OR 2 CYCLES.
- ABILITY TO MAINTAIN OPERATION DURING IDLE MODE @ 2.7 V
- EXIT IDLE MODE WITH AN EXTERNAL INTERRUPT SIGNAL OR RESET SIGNAL
- 100 % STATIC OPERATION FROM DC TO 6 MHz
- BATTERY OPERATION
- 2 POWER CONSUMPTION SELECTIONS
  - NORMAL OPERATION : < 2 mA/MHz @ 5.5 V
  - IDLE MODE : < 10 µA @ 5.5 V
- TTL COMPATIBLE OPERATIONS : Vcc = 5 V ± 10 %
  CMOS COMPATIBLE OPERATION AS AN OPTION Vcc = 5 V ± 20 %

MHS' 80C48/80C35 are low-power versions of the popular 8048H/8035HL microcomputers. By using its well known SAJI IV CMOS technology in the design of these devices, MHS provides microcomputers with low power consumption and high performance.

The 80C48 contains a 1K × 8 program memory, a 64 × 8 RAM data memory, 27 I/O lines, and a 8-bit timer/counter in addition to an on-board oscillator and clock circuits. For systems that require extra capability, the 80C48 can be expanded using CMOS external memories and MCS-80® and MCS-85® peripherals of MHS 82C43 I/O expander. The 80C35 is the equivalent of the 80C48 without program memory on-board.

The SAJI IV design of the 80C48 opens new applications areas that require battery operation, low power standby, wide voltage range, and the ability to maintain operation during IDLE mode. These applications include portable and handheld instruments, telecommunications, consumer and automotive.

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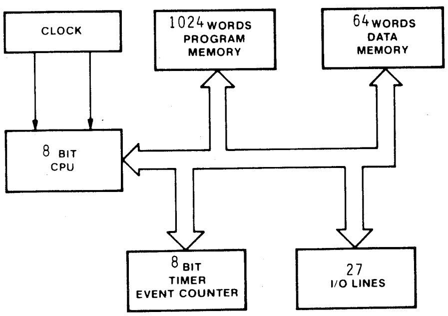


Figure 1.
Block Diagram

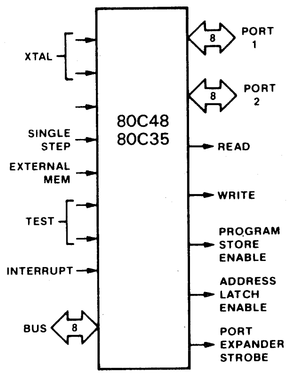


Figure 2.
Logic Symbol

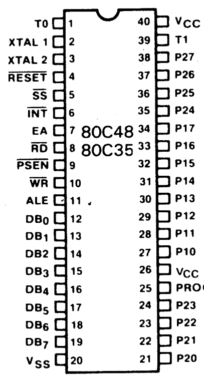


Figure 3.
Pin Configuration

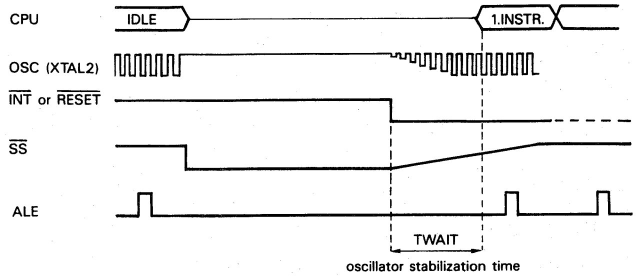
Table 1. Pin Description

Symbol	Pin No.	Function
V_{SS}	20	Circuit GND potential
V_{CC}	40-26	Main power supply; + 5 V during operation. Pins 40 and 26 are internally connected.
$\overline{PROG}$	25	Output strobe for 8243 or 82C43 I/O expander.
P10-P17 Port 1	27-34	8-bit quasi-bidirectional port.
P20-P27 Port 2	21-24 35-38	8-bit quasi-bidirectional port. P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243 or 82C43.
DB0-DB7 BUS	12-19	True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.
T0	1	Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction.
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.
$\overline{INT}$	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low) Interrupt must remain low for at least 3 machine cycles to ensure proper operation. Interrupt is also used to exit IDLE mode.

Symbol	Pin No.	Function
$\overline{RD}$	8	Output strobe activated during a BUS read. Can be used to enable data onto the bus from an external device. Used as a read strobe to external data memory. (Active low)
$\overline{RESET}$	4	Input which is used to initialize the processor. (Active low) (Non TTL V_{IH}). Reset is also used to exit IDLE mode.
$\overline{WR}$	10	Output strobe during a bus write. (Active low) Used as write strobe to external data memory.
ALE	11	Address latch enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.
$\overline{PSEN}$	9	Program store enable. This output occurs only during a fetch to external program memory. (Active low)
$\overline{SS}$	5	Single step input. Can be used in conjunction with ALE to 'single step' the processor through each instruction. (Active low) If IDLE MODE operation is required, a capacitor must be applied between $\overline{SS}$ and V_{SS} allowing oscillator stabilization upon IDLE exit. (C_{SS} min = 20 nF)
EA	7	If not connected, internally forced at Vcc. This input pin (Non TTL input) is useful for emulation and debug and essential for testing and program verification - At Vcc : External access input which forces all program memory fetches to reference external memory (80C35 normal operation). - At Vss : The 1st Kbyte of memory is in internal access mode. (80C48 normal operation). - At Vcc/2 : Selects the program memory verification mode.
XTAL1	2	Input to internal oscillator. One side of crystal/external source input.
XTAL2	3	Output from internal oscillator. Other side of crystal/external source input.

Idle mode description

To place the 80C48/80C35 in the IDLE MODE, a command instruction 'IDLE' (op code 01_H) is executed.
In the IDLE MODE, the microcontroller is completely stopped (including oscillator) and its supply current is very low (refer IIDLE parameter). This mode stops oscillator and maintains the internal register, RAM and Data I/O in the state they were before IDLE instruction. These informations can be maintained at Vcc = 2.7 V.
The 80C48/80C35 exits IDLE MODE by receiving a hard RESET or an external interrupt. Then the oscillator restarts and will be stabilized after T_{WAIT} delay. The external capacitor Css applied on $\overline{SS}$ pin is loaded thru an ≈ 100 KΩ internal resistor R thus generating a delay (T_{WAIT} = RC_{SS}). Then the 80C48/80C35 can execute instructions as shown hereafter.



Idle functionnal diagram

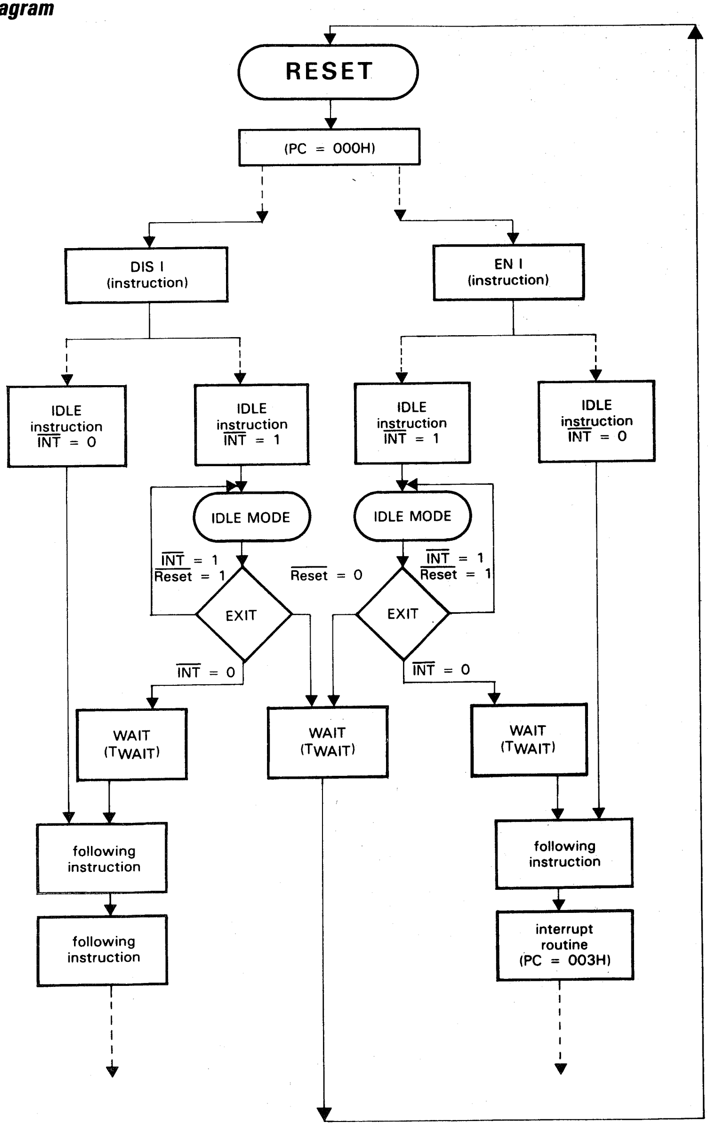


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Table 2. **Instruction Set**

Mnemonic	Function	Description	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	C	AC	F0	F1
			Instruction Code										Flags			
Accumulator																
ADD, A = data	(A) ← (A) + data	Add immediate the specified Data to the Accumulator.	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•			
Add A, Rr	(A) ← (A) + (Rr) for r = 0 - 7	Add contents of designated register to the Accumulator.	0	1	1	0	1	r	r	r	1	1	•			
ADD A, @ Rr	(A) ← (A) + ((Rr)) for r = 0 - 1	Add indirect the contents of the data memory location to the Accumulator.	0	1	1	0	0	0	0	r	1	1	•			
ADDC A, = data	(A) ← (A) + (C) + data	Add immediate with carry the specified data to the Accumulator.	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•			
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0 - 7	Add with carry the contents of the designated register to the Accumulator.	0	1	1	1	1	r	r	r	1	1	•			
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0 - 1	Add indirect with carry the contents of data memory location to the Accumulator.	0	1	1	1	0	0	0	r	1	1	•			
ANL A, = data	(A) ← (A) AND data	Logical AND specified immediate Data with Accumulator.	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0 - 7	Logical AND contents of designated register with Accumulator.	0	1	0	1	1	r	r	r	1	1				
ANL A, @ Rr	(A) ← (A) AND ((Rr)) for r = 0 - 1	Logical AND indirect the contents of data memory with Accumulator.	0	1	0	1	0	0	0	r	1	1				
CPL A	(A) ← NOT (A)	Complement the contents of the Accumulator.	0	0	1	1	0	1	1	1	1	1				
CLR A	(A) ← 0	Clear the contents of the Accumulator.	0	0	1	0	0	1	1	1	1	1				
DA A		Decimal Adjust the contents of the Accumulator.	0	1	0	1	0	1	1	1	1	1	•			
DEC A	(A) ← (A) 1	Decrement by 1 the Accumulator's contents.	0	0	0	0	0	1	1	1	1	1				
INC A	(A) ← (A) + 1	Increment by 1 the Accumulator's contents.	0	0	0	1	0	1	1	1	1	1				
ORL A, = data	(A) ← (A) OR data	Logical OR specified immediate data with Accumulator.	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0 - 7	Logical OR contents of designated register with Accumulator.	0	1	0	0	1	r	r	r	1	1				
ORL A, @ Rr	(A) ← (A) OR ((Rr)) for r = 0 - 1	Logical OR indirect the contents of data memory location with Accumulator.	0	1	0	0	0	0	0	r	1	1				
RL A	(AN + 1) ← (AN) (A_0) ← (A_7) for N = 0 - 6	Rotate Accumulator left by 1 bit without carry.	1	1	1	0	0	1	1	1	1	1				
RLC A	(AN + 1) ← (AN); N = 0 - 6 (A_0) ← (C) (C) ← (A_7)	Rotate Accumulator left by 1 bit through carry.	1	1	1	1	0	1	1	1	1	1	•			
RR A	(AN) ← (AN + 1), N = 0 - 6 (A_7) ← (A_0)	Rotate Accumulator right by 1 bit without carry.	0	1	1	1	0	1	1	1	1	1				
RRC A	(AN) ← (AN + 1); N = 0 - 6 (A_7) ← (C) (C) ← (A_0)	Rotate Accumulator right by 1 bit through carry.	0	1	1	0	0	1	1	1	1	1	•			
SWAP A	(A_{4-7}) ⇄ (A_0-3)	Swap the two 4-bit nibbles in the Accumulator.	0	1	0	0	0	1	1	1	1	1				
XRL A, = data	(A) ← (A) XOR data	Logical XOR specified immediate data with Accumulator.	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0 - 7	Logical XOR contents of designated register with Accumulator.	1	1	0	1	1	r	r	r	1	1				
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0 - 1	Logical XOR indirect the contents of data memory location with Accumulator.	1	1	0	1	0	0	0	r	1	1				
Branch																
DJNZ Rr, addr	(Rr) ← (Rr) - 1; r = 0 - 7 If (Rr) ≠ 0 (PC 0 - 7) ← addr	Decrement the specified register and test contents.	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2				
JBb addr	(PC 0 - 7) ← addr if Bb = 1 (PC) - (PC) + 2 if Bb = 0	Jump to specified address if Accumulator bit is set.	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2				
JC addr	(PC 0 - 7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF 0 addr	(PC 0 - 7) ← addr if FO = 1 (PC) ← (PC) + 2 if FO = 0	Jump to specified address if Flag F 0 is set.	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF 1 addr	(PC 0 - 7) ← addr if F 1 = 1 (PC) ← (PC) + 2 if F 1 = 0	Jump to specified address if Flag F 1 is set.	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JMP addr	(PC 8 - 10) ← addr 8 – 10 (PC 0 - 7) ← addr 0 - 7 (PC 11) ← DBF	Direct Jump to specified address within the 2K address block.	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2				
JMPP @ A	(PC 0 7) ← ((A))	Jump indirect to specified address with address page.	1	0	1	1	0	0	1	1	2	1				
JNC addr	(PC 0 7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNI addr	(PC 0 7) ← addr if I = 0 (PC) ← (PC) + 2 if = 1	Jump to specified address if interrupt is low.	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				

Instruction Set (Cont.)

Mnemonic	Function	Description	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	C	AC	F0	F1
			Instruction Code										Flags			
		Branch (Cont.)														
JNT0 addr	(PC 0 - 7) ← addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if Test 0 is low.	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNT1 addr	(PC 0 - 7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if Test 1 is low.	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNZ addr	(PC 0 - 7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 0	Jump to specified addres if Accumulator is non-zero.	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JTF addr	(PC 0 - 7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if Timer Flag is set to 1.	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT0 addr	(PC 0 - 7) ← addr if T0 = 1 (PC) ← (PC) + 2 if T0 = 0	Jump to specified address if Test 0 is a 1.	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT1 addr	(PC 0 - 7) ← addr if T1 = 1 (PC) ← (PC) - 2 if T1 = 0	Jump to specified address if Test 1 is a 1.	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JZ addr	(PC 0 - 7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if Accumulator is 0.	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
		Control														
EN I		Enable the External Interrupt input.	0	0	0	0	0	1	0	1	1	1				
DIS I		Disable the External Interrupt input.	0	0	0	1	0	1	0	1	1	1				
ENT0 CLK		Enable the Clock Output pin T0.	0	1	1	1	0	1	0	1	1	1				
SEL MB0	(DBF) ← 0	Select Bank 0 (locations 0 - 2047) of Program Memory.	1	1	1	0	0	1	0	1	1	1				
SEL MB1	(DBF) ← 1	Select Bank 1 (locations 2048 - 4095) of Program Memory.	1	1	1	1	0	1	0	1	1	1				
SEL RB0	(BS) ← 0	Select Bank 0 (locations 0 - 7) of Data Memory.	1	1	0	0	0	1	0	1	1	1				
SEL RB1	(BS) ← 1	Select Bank 1 (locations 24 - 31) of Data Memory.	1	1	0	1	0	1	0	1	1	1				
		Data Moves														
MOV A, = data	(A) ← data	Move Immediate the specified data into the Accumulator.	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
MOV A, Rr	(A) ← (Rr); r = 0 - 7	Move the contents of the designated registers into the Accumulator.	1	1	1	1	1	r	r	r	1	1				
MOV A, @ Rr	(A) ← ((Rr)); r = 0 - 1	Move Indirect the contents of data memory location into the Accumulator.	1	1	1	1	0	0	0	r	1	1				
MOV A, PSW	(A) ← (PSW)	Move contents of the Program Status Word into the Accumulator.	1	1	0	0	0	1	1	1	1	1				
MOV Rr, = data	(Rr) ← data; r = 0 - 7	Move Immediate the specified data into the designated register.	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2				
MOV Rr, A	(Rr) ← (A); r = 0 - 7	Move Accumulator Contents into the designated register.	1	0	1	0	1	r	r	r	1	1				
MOV @ Rr, A	((Rr)) ← (A), r = 0 - 1	Move Indirect Accumulator Contents into data memory location.	1	0	1	0	0	0	0	r	1	1				
MOV @ Rr, = data	((Rr)) ← data; r = 0 - 1	Move Immediate the specified data into data memory.	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2				
MOV PSW, A	(PSW) ← (A)	Move contents of Accumulator into the program status word.	1	1	0	1	0	1	1	1	1	1				
MOVP A, @ A	(PC 0 - 7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator.	1	0	1	0	0	0	1	1	2	1				
MOVP3 A, @ A	(PC 0 - 7) ← (A) (PC 8 - 10) ← 011 (A) ← ((PC))	Move Program data in Page 3 into the Accumulator.	1	1	1	0	0	0	1	1	2	1				
MOVX A, @ R	(A) ← ((Rr)); r = 0 - 1	Move Indirect the contents of external data memory into the Accumulator.	1	0	0	0	0	0	0	r	2	1				
MOVX @ R, A	((Rr)) ← (A), r = 0 - 1	Move Indirect the contents of the Accumulator into external data memory.	1	0	0	1	0	0	0	r	2	1				
XCH A, Rr	(A) ⇄ (Rr); r = 0 - 7	Exchange the Accumulator and designated register's contents.	0	0	1	0	1	r	r	r	1	1				
XCH A, @ Rr	(A) ← ((Rr)); r = 0 - 1	Exchange Indirect contents of Accumulator and location in data memory.	0	0	1	0	0	0	0	r	1	1				
XCHD A, @ Rr	(A 0 - 3) ⇄ ((Rr)) 0 - 3)); r = 0 - 1	Exchange Indirect 4 bit contents of Accumulator and data memory.	0	0	1	1	0	0	0	r	1	1				
		Flags														
CPL C	(C) ← NOT (C)	Complement carry bit.	1	0	1	0	0	1	1	1	1	1	•			
CPL F0	(F0) ← NOT (F0)	Complement Flag F0.	1	0	0	1	0	1	0	1	1	1			•	
CPL F1	(F1) ← NOT (F1)	Complement of Flag F 1.	1	0	1	1	0	1	0	1	1	1				•
CLR C	(C) ← 0	Clear carry bit to 0.	1	0	0	1	0	1	1	1	1	1	•			
CLR F0	(F0) ← 0	Clear Flag 0 to 0.	1	0	0	0	0	1	0	1	1	1			•	
CLR F1	(F1) ← 0	Clear Flag 1 to 0.	1	0	1	0	0	1	0	1	1	1				•

4

Instruction Set (Cont.)

Mnemonic	Function	Description	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	C	AC	F0	F1
Input/Output																
ANL BUS, data	(BUS) ← (BUS) AND data	Logical AND immediate specified data with contents of Bus.	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2				
ANL P_p, data	(P_p) ← (P_p) AND data p 1 - 2	Logical AND immediate specified data with designated port (1 or 2).	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2				
ANLD P_p, A	(P_p) ← (P_p) AND (A0 - 3) p 4 - 7	Logical AND contents of Accumulator with designated port (4 - 7).	1	0	0	1	1	1	p	p	2	1				
IN A, P_p	(A) ← (P_p), p 1 - 2	Input data from designated port (1 - 2) into Accumulator.	0	0	0	0	1	0	p	p	2	1				
INS A, BUS	(A) ← (BUS)	Input strobed Bus data into Accumulator.	0	0	0	0	1	0	0	0	2	1				
MOVD A, P_p	(A 0 - 3) ← (P_p); p = 4 - 7 (A 4 - 7) ← 0	Move contents of designated port (4 - 7) into Accumulator.	0	0	0	0	1	1	p	p	2	1				
MOVD P_p, A	(P_p) ← A 0 - 3; p = 4 - 7	Move contents of Accumulator designated port (4 - 7).	0	1	1	1	1	p	p	1	1					
ORL BUS, = data	(BUS) ← (BUS) OR data	Logical OR immediate specified data with contents of Bus.	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2				
ORLD P_p, A	(P_p) ← (P_p) OR (A0 - 3) P = 4 - 7	Logical OR contents of Accumulator with designated port (4 - 7).	1	0	0	0	1	1	p	p	1	1				
ORL P_p, = data	(P_p) ← (P_p) OR data p = 1 - 2	Logical OR immediate specified data with designated port (1 - 2).	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2				
OUTL BUS, A	(BUS) ← (A)	Output contents of Accumulator onto Bus.	0	0	0	0	0	0	1	0	1	1				
OUTL P_p, A	(P_p) ← (A); p = 1 - 2	Output contents of Accumulator to designated port (1 - 2).	0	0	1	1	1	0	p	p	1	1				
Registers																
DEC Rr (Rr)	(Rr) ← (Rr) 1; r = 0 - 7	Decrement by 1 contents of designated register.	1	1	0	0	1	r	r	r	1	1				
INC Rr	(Rr) ← (Rr) + 1, r = 0 - 7	Increment by 1 contents of designated register.	0	0	0	1	1	r	r	r	1	1				
INC @ R	((Rr)) ← ((Rr)) + 1; r = 0 - 1	Increment Indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r	1	1				
Subroutine																
Call addr	((SP)) ← (PC), (PSW 4 - 7) (SP) ← (SP) + 1 (PC 8 - 10) ← addr 8 - 10 (PC 0 - 7) ← addr 0 - 7 (PC 11) ← DBF	Call designated Subroutine.	a_{10} a_7	a_9 a_6	a_8 a_5	1 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2				
RET	(SP) ← (SP) 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word.	1	0	0	0	0	0	1	1	2	1				
RETR	(SP) ← (SP) 1 (PC) ← ((SP)) (PSW 4 - 7) ← ((SP))	Return from Subroutine restoring Program Status Word.	1	0	0	1	0	0	1	1	2	1				
Timer/Counter																
EN TCNTI		Enable Internal interrupt Flag for Timer/Counter output.	0	0	1	0	0	1	0	1	1	1				
DIS TCNTI		Disable Internal interrupt Flag for Timer/Counter output.	0	0	1	1	0	1	0	1	1	1				
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator.	0	1	0	0	0	0	1	0	1	1				
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/Counter.	0	1	1	0	0	0	1	0	1	1				
STOP TCNT		Stop Count for Event Counter	0	1	1	0	0	1	0	1	1	1				
STRT CNT		Start Count for Event Counter	0	1	0	0	0	1	0	1	1	1				
STRT T		Start Counter for Timer.	0	1	0	1	0	1	0	1	1	1				
Miscellaneous																
NOP		No Operation performed.	0	0	0	0	0	0	0	0	1	1				
IDLE		Select Idle operation	0	0	0	0	0	0	0	1	1	1				

Notes:

1. Instruction Code Designations r and p form the binary representation of the Registers and Ports involved.
2. The dot under the appropriate flag bit indicates that its content is subject to change by the instruction it appears in.
3. References to the address and data are specified in bytes 2 and/or 1 of the instruction.
4. Numerical Subscripts appearing in the FUNCTION column reference the specific bits affected.

Symbol Definitions:

SYMBOL	DESCRIPTION
A	The Accumulator
AC	The Auxiliary Carry Flag
addr	Program Memory Address (12 bits)
Bb	Bit Designator (b = 0 – 7)
BS	The Bank Switch
BUS	The BUS Port
C	Carry Flag
CLK	Clock Signal
CNT	Event Counter
D	Nibble Designator (4 bits)
data	Number or Expression (8 bits)
DBF	Memory Bank Flip-Flop
F_0, F_1	Flags 0, 1
I	Interrupt
P	"In-Page" Operation Designator

SYMBOL	DESCRIPTION
P_p	Port Designator (p = 1, 2 or 4 – 7)
PSW	Program Status Word
Rr	Register Designator (r = 0, 1 or 0 – 7)
SP	Stack Pointer
T	Timer
TF	Timer Flag
T_0, T_1	Testable Flags 0, 1
X	External RAM
=	Prefix for Immediate Data
@	Prefix for Indirect Address
S	Program Counter's Current Value
(x)	Contents of External RAM Location
((x))	Contents of Memory Location Addressed by the Contents of External RAM Location
←	Replaced By

4

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . 0° C to 70° C
Storage Temperature . . . . – 65° C to + 125° C
Voltage On Any Pin With Respect
to Ground . . . . – 0,5 V to Vcc + 0.5 V
Power Dissipation . . . . 0.5 Watt

**NOTICE : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

80C48/35 COMMERCIAL TEMPERATURE RANGE

D.C. CHARACTERISTICS (TA = 0° C to 70° C, VCC = 5 V ± 10 %, VSS = 0 V); TTL COMPATIBLE VERSION)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
VIL	Input Low Voltage (All Except $\overline{RESET}$, XI, X2, EA)	– .5		.8	V	
VIL1	Input Low Voltage ($\overline{RESET}$, X1, X2, EA)	– .5		.6	V	
VIH	Input High Voltage (All Except XTAL1, XTAL2, $\overline{RESET}$, EA)	VCC–2		VCC+0.5V	V	
VIH1	Input High Voltage (X1, X2, $\overline{RESET}$, EA)	VCC–1		VCC+0.5V	V	
VOL	Output Low Voltage (BUS)		0.2	.45	V	IOL = 2.0 mA
VOL1	Output Low Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)		0.2	.45	V	IOL = 1.8 mA
VOL2	Output Low Voltage (PROG)		0.2	.45	V	IOL = 1.0 mA
VOL3	Output Low Voltage (All Other Outputs)		0.2	.45	V	IOL = 1.6 mA
VOH	Output High Voltage (BUS)	VCC- 0.5			V	IOH = – 400 μA
VOH1	Output High Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	VCC -0.5			V	IOH = – 100 μA
VOH2	Output High Voltage (All Other Outputs)	VCC -0.5			V	IOH = – 40 μA
IL1	Input Leakage Current (T1, $\overline{INT}$)			± 10	μA	VSS≤VIN≤VCC
ILI1	Input Current (P10-P17, P20-P27, EA, SS)			– 500	μA	VSS≤VIN≤VCC
ILO	Output Leakage Current (BUS, TO) (High Impedance State)			± 10	μA	VSS≤VIN≤VCC
ICC	Supply Current			10 3	mA mA	VIN = VCC or VSS f = 6 MHz Outputs Open f = 1 MHz Outputs Open
IIDLE	Idle Mode Current		10	50	μA	Outputs Open

TA = 0° C to 70° C VCC = 2.7 V to 5.5 V VSS = 0 V

VIL	Input Low Voltage	– .3		0.18 VCC	V	
VIL1	Input Low Voltage ($\overline{RESET}$, X1, X2, EA)			0.13 VCC	V	
VIH	Input High Voltage	0.7 VCC			V	
VIH1	Input High Voltage ($\overline{RESET}$, X1, X2, EA)	0.75 VCC			V	
VOL	Output Low Voltage			0.1 VCC	V	IOL = 1 mA
VOH	Output High Voltage (BUS)	0.9 VCC			V	IOH = – 100 μA
VOH1	Output High Voltage (Others Outputs)	0.9 VCC			V	IOH = – 10 μA

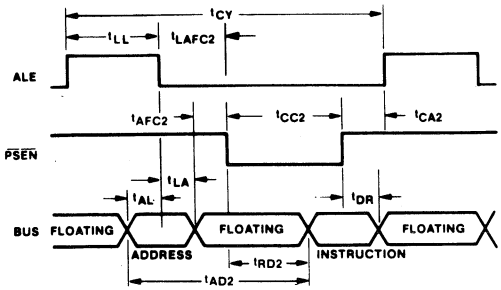
A.C. CHARACTERISTICS (T_A = 0° C to 70° C, V_{CC} = 5 V ± 10 %, V_{SS} = 0 V) (Note 6)

Symbol	Parameter	Approximate formula gate delay not included f (tCY)	6 MHz Min	6 MHz Max	Unit	Conditions (Note 1)
tLL	ALE Pulse Width	7/30 tCY – 170	400		ns	
tAL	Addr. Setup to ALE	1/5 tCY – 110	120		ns	
tLA	Addr. Hold from ALE	1/15 tCY – 40	80		ns	
tCC1	Control Pulse Width ($\overline{RD}$, $\overline{WR}$)	1/2 tCY – 200	700		ns	
tCC2	Control Pulse Width ($\overline{PSEN}$)	2/5 tCY – 200	700		ns	
tDW	Data Setup before $\overline{WR}$	15/30 tCY – 200	500		ns	
tWD	Data Hold after $\overline{WR}$	1/10 tCY – 50	80		ns	(Note 2)
tDR	Data Hold ($\overline{RD}$, $\overline{PSEN}$)	1/10 tCY – 30	0	200	ns	
tRD1	$\overline{RD}$ to Data in	2/5 tCY – 200		500	ns	
tRD2	$\overline{PSEN}$ to Data in	3/10 tCY – 200		500	ns	
tAW	Addr. Setup to $\overline{WR}$	2/5 tCY – 150	230		ns	
tAD1	Addr. Setup to Data ($\overline{RD}$)	24/30 tCY – 250		950	ns	
tAD2	Addr. Setup to Data ($\overline{PSEN}$)	3/5 tCY – 250		950	ns	
tAFC1	Addr. Float to $\overline{RD}$, $\overline{WR}$	2/15 tCY – 40	0		ns	
tAFC2	Addr. Float to $\overline{PSEN}$	1/30 tCY – 40	0		ns	
tLAFC1	ALE to Control, ($\overline{RD}$, $\overline{WR}$)	1/5 tCY – 75	420		ns	
tLAFC2	ALE to Control ($\overline{PSEN}$)	1/10 tCY – 75	170		ns	
tCA1	Control to ALE ($\overline{RD}$, $\overline{WR}$, $\overline{PROG}$)	1/15 tCY – 40	10		ns	
tCA2	Control to ALE ($\overline{PSEN}$)	4/15 tCY – 40	50		ns	
tCP	Port Control Setup to $\overline{PROG}$	1/10 tCY – 80	100		ns	
tPC	Port Control Hold to $\overline{PROG}$	4/15 tCY – 200	140		ns	
tPR	$\overline{PROG}$ to P2 Input Valid	6/10 tCY – 120		810	ns	
tPF	Input Data Hold from $\overline{PROG}$	1/10 tCY	0	150	ns	
tDP	Output Data Setup	2/5 tCY – 150	250		ns	
tPD	Output Data Hold	1/10 tCY – 50	65		ns	
tPP	$\overline{PROG}$ Pulse Width	7/10 tCY – 250	1200		ns	
tPL	Port 2 I/O Setup to ALE	4/15 tCY – 200	350		ns	
tLP	Port 2 I/O Hold to ALE	2/15 tCY – 100	150		ns	
tPV	Port Output from ALE	3/10 tCY + 100		850	ns	
tCY	Cycle Time	15/fXTAL	2.5 (note 4)		µs	
t0PRR	T0 Rep Rate	3/15 tCY	500		ns	
tWAIT	Oscillator Stabilization Time after IDLE Mode Exit (Note 5)		typ : 2 typ : 10		ms ms	CSS = 20 nF CSS = 100 nF

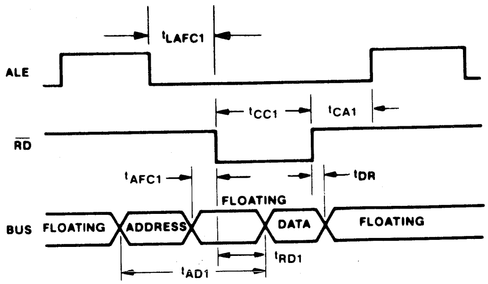
Notes :

1. Control Outputs CL = 80 pF
   BUS Outputs CL = 150 pF
2. BUS High Impedance Load 20 pF
3. Interrupt pin must remain low for at least 3 tCY to ensure proper operation.
4. Corresponds to 6 MHz XTAL
5. Not 100 % tested
6. The 80C48/80C35 is guaranteed
   with VCC = 5 V ± 10 % at 6 MHz
   with VCC = 3 to 5.5 V at 1 MHz

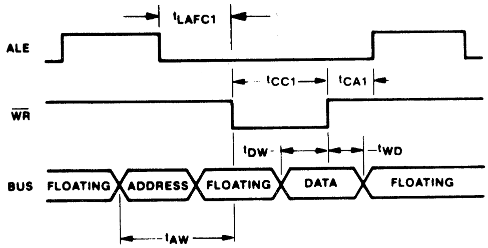
WAVEFORMS



Instruction Fetch From External Program Memory

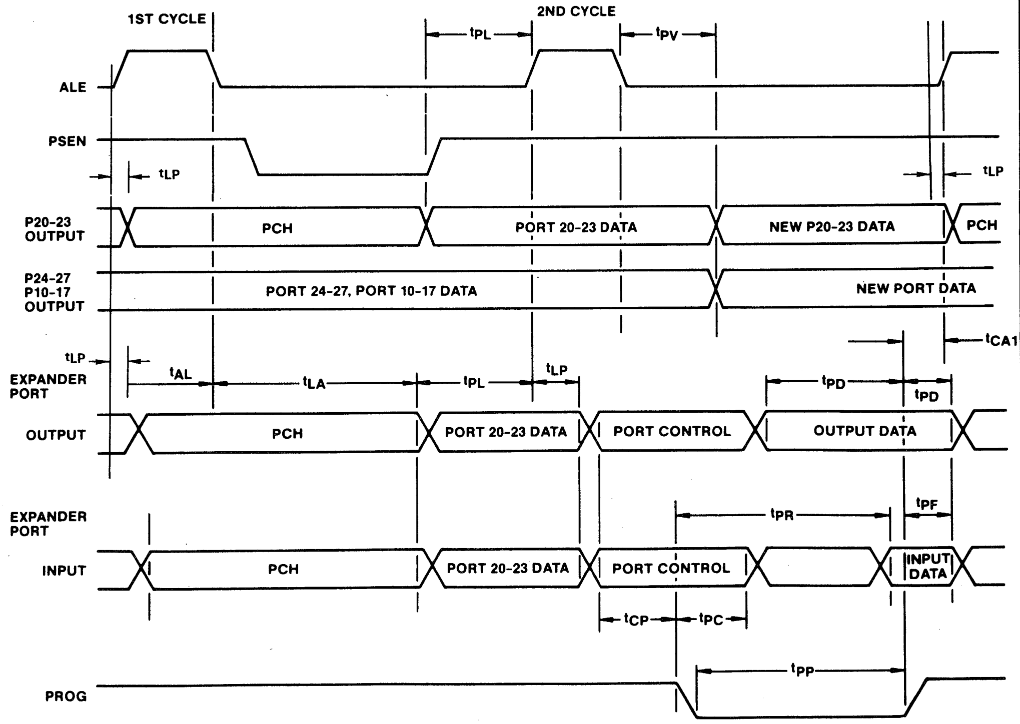


Read From External Data Memory



Write to External Data Memory

PORT 1/PORT 2 TIMING



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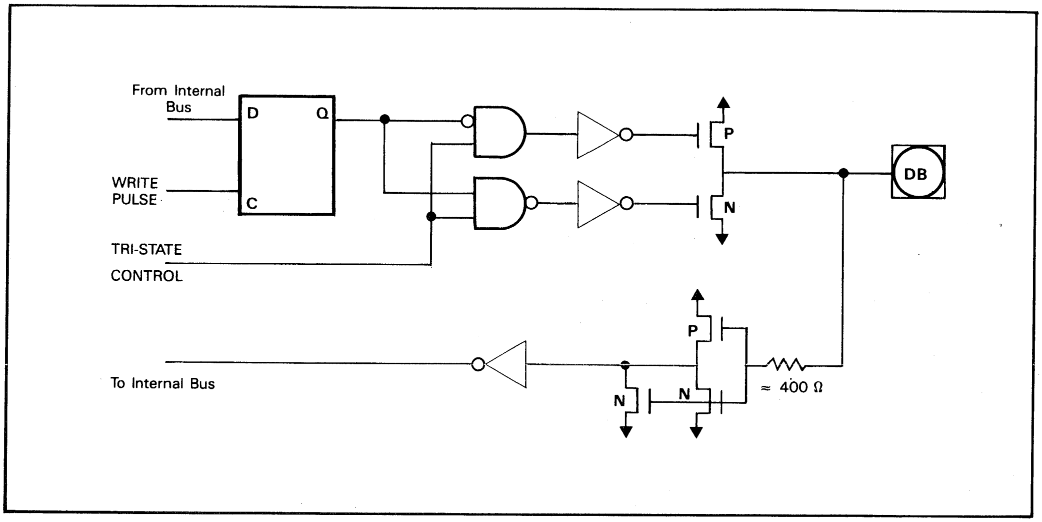
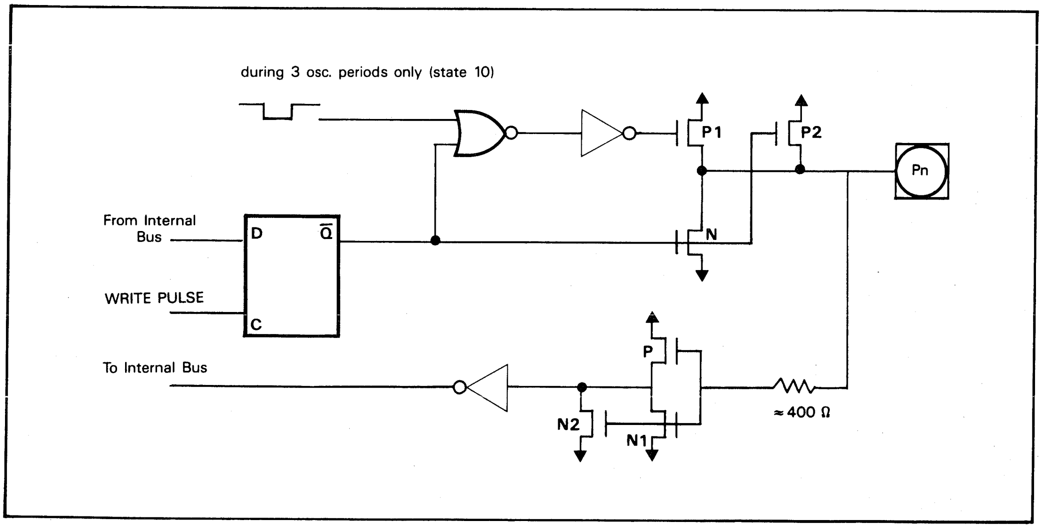
BUS PORT CONFIGURATION

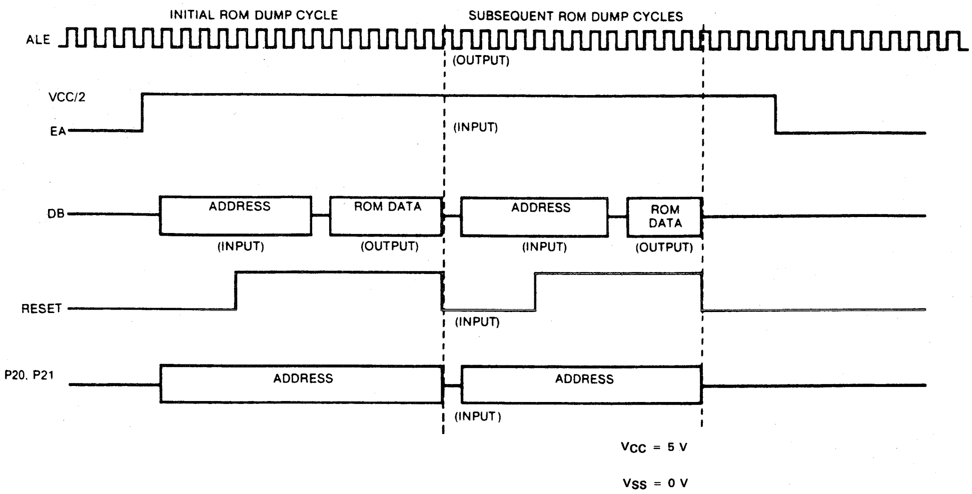


PORTS 1 & 2 CONFIGURATION

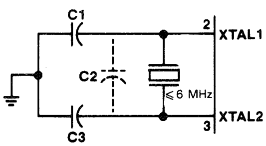


When a '1' level is written on ports, PMOS 1 is turned on for 3 osc. periods after Q makes a 1-to-0 transition; PMOS 2 (weak pull-up transistor) is ON.

SUGGESTED ROM VERIFICATION ALGORITHM



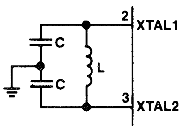
OSCILLATOR MODE



C1 = 5pF ± 1/2pF + STRAY < 5pF
C2 = CRYSTAL + STRAY < 8pF
C3 = 20pF ± 1pF + STRAY < 5pF

CRYSTAL SERIES RESISTANCE SHOULD BE LESS THAN 75 Ω AT 6MHz; LESS THAN 180 Ω AT 3.6MHz.

LC OSCILLATOR MODE



$f \approx \frac{1}{2\pi\sqrt{LC'}}$

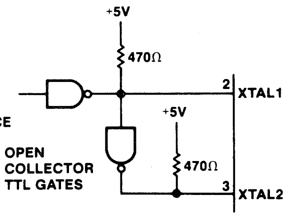
$C' = \frac{C + 3C_{pp}}{2}$

$C_{pp} \approx$ 5-10 pF PIN-TO-PIN CAPACITANCE

L	C	NOMINAL 1
45 µH	20pF	5.2 MHz
120µH	20pF	3.2 MHz

EACH C SHOULD BE APPROXIMATELY 20pF, INCLUDING STRAY CAPACITANCE.

DRIVING FROM EXTERNAL SOURCE



OPEN COLLECTOR TTL GATES

FOR THE 80C48 XTAL1 MUST BE HIGH 35-65 % OF THE PERIOD AND XTAL2 MUST BE HIGH 35-65 % OF THE PERIOD. RISE AND FALL TIMES MUST NOT EXCEED 20ns.

Ordering Information

MHS Part Number	Package	Temperature Range	Notes
P... - 80C48 nn	Plastic	0° C - 70° C Commercial	1K byte Mask Programmable ROM
D... - 80C48 nn	Cerdip	0° C - 70° C ″	″
XX.. - 80C48 nn	Dice in Chip tray	Probed at 25° C ″	″
P... - 80C35	Plastic	0° C - 70° C ″	ROM less version
D... - 80C35	Cerdip	″ ″	″
XX.. - 80C35	Dice in Chip tray	Probed at 25° C ″	″

nn is ROM code P/N.

MATRA-HARRIS SEMICONDUCTEURS

data sheet

82C43
CMOS INPUT/OUTPUT EXPANDER FOR MCS 48® FAMILY

ADVANCE INFORMATION

4

Features

- LOW COST
- SIMPLE INTERFACE TO MCS-48® MICROCOMPUTERS (80C48, 8048, 8041, 8051...)
- FOUR 4-BIT I/O PORTS
- "AND"AND"OR"DIRECTLY TO PORTS
- 24-PIN DIP CERDIP OR PLASTIC
- SINGLE 5V SUPPLY
- HIGH OUTPUT DRIVE
- DIRECT EXTENSION OF RESIDENT 8048 - 80C48 I/O PORTS
- HIGH NOISE IMMUNITY - TYPICALLY 33 %

Description

The MHS 82C43 is a C-MOS input/output expander designed specifically to provide a low cost means of I/O expansion for the MCS-48® family of single chip microcomputers. Fabricated in MHS scaled saji 4 C-MOS 82C43 process combines low cost, single supply voltage and high drive current capability.

The MHS 82C43 consists of four 4-bit bidirectional static I/O ports and one 4-bit port which serves as an interface to the MCS-48 microcomputers. The 4-bit interface requires that only 4 I/O lines of the 80C48 be used for I/O expansion, and also allows multiple 82C43's to be added to the same bus.

The I/O ports of the 82C43 serve as a direct extension of the resident I/O facilities of the MCS-48 microcomputers and are accessed by their own MOV, ANL, and ORL instructions.

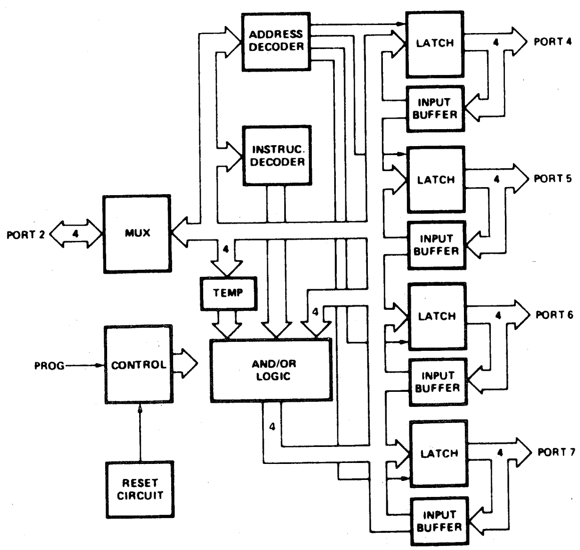


Figure 1. 82C43 Block Diagram

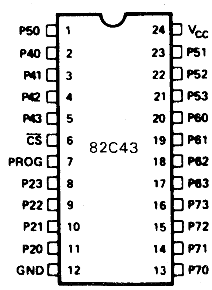


Figure 2. 82C43 Pin Configuration

® TRADEMARK OF INTEL CORPORATION

Table 1. Pin Description

Symbol	Pin No.	Function
PROG	7	Clock Input. A high to low transition on PROG signifies that address and control are available on P20-P23, and a low to high transition signifies that data is available on P20-P23.
$\overline{CS}$	6	Chip Select Input. A high on CS inhibits any change of output or internal status.
P20-P23	11-8	Four (4) bit bi-directional port contains the address and control bits on a high to low transition of PROG. During a low to high transition contains the data for a selected output port if a write operation, or the data from a selected port before the low to high transition if a read operation.
GND	12	0 volt supply.
P40-P43 P50-P53 P60-P63 P70-P73	2-5 1, 23-21 20-17 13-16	Four (4) bit bi-directional I/O ports. May be programmed to be input (during read), low impedance latched output (after write), or a tri-state (after read). Data on pins P20-P23 may be directly written, ANDed or ORed with previous data.
V_{CC}	24	+5 volt supply.

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FUNCTIONAL DESCRIPTION

General Operation

The 82C43 contains four 4-bit I/O ports which serve as an extension of the on-chip I/O and are addressed as ports 4-7. The following operations may be performed on these ports:

- Transfer Accumulator to Port.
- Transfer Port to Accumulator.
- AND Accumulator to Port.
- OR Accumulator to Port.

All communication between the microcomputer and the 82C43 occurs over Port 2 (P20-P23) with timing provided by an output pulse on the PROG pin of the processor. Each transfer consists of two 4-bit nibbles :

The first containing the "op code" and port address and the second containing the actual 4-bits of data. A high to low transition of the PROG line indicates that address is present while a low to high transition indicates the presence of data. Additional 82C43's may be added to the 4-bit bus and chip selected using additional output lines from the 8048/8748/8031/8035/80C48/80C35/8051.

Power On Initialization

Initial application of power to the device forces input/output ports 4, 5, 6, and 7 to the tri-state and port 2 to the input mode. The PROG pin may be either high or low when power is applied. The first high to low transition of PROG causes device to exit power on mode. The power on sequence is initiated if VCC drops below 1V. This power on initialization is guaranted to be compatible with MCS 48® (i.e. $\leqslant$10 ms). Typical value is $<$ 5 ms.

P21	P20	Address Code	P23	P22	Instruction Code
0	0	Port 4	0	0	Read
0	1	Port 5	0	1	Write
1	0	Port 6	1	0	ORLD
1	1	Port 7	1	1	ANLD

During power-on a soft pull-down (50 µA max.) is activated in order not to let the output floating as it is in the full tri-state mode. The first time a port is adressed the pull-down is de-activated.

Write Modes

The device has three write modes. MOVD Pi, A directly writes new data into the selected port and old data is lost. ORLD Pi, A takes new data, OR's it with the old data and then writes it to the port. ANLD Pi, A takes new data, AND's it with the old data and then writes it to the port. Operation code and port address are latched from the input port 2 on the high to low transition of the PROG pin. On the low to high transition of PROG data on port 2 is transferred to the logic block of the specified output port.

After the logic manipulation is performed, the data is latched and outputed. The old data remains latched until new valid outputs are entered.

Read Mode

The device has one read mode. The operation code and port address are latched from the input port 2 on the high to low transition of the PROG pin. As soon as the read operation and port address are decoded, the appropriate outputs are tri-stated, and the input buffers switched on. The read operation is terminated by a low to high transition of the PROG pin. The port (4, 5, 6 or 7) that was selected is switched to the tri-stated mode while port 2 is returned to the input mode.

Normally, a port will be in an output (write mode) or input (read mode). If modes are changed during operation, the first read following a write should be ignored; all following reads are valid. This is to allow the external driver on the port to settle after the first read instruction removes the low impedance drive from the 82C43 output. A read of any port will leave that port in a high impedance state.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . . 0° C to 70° C
Storage Temperature . . . . -65° C to +150° C
Voltage on Any Pin With
Respect to Ground . . . . Ground -0,5V to V_{CC} +0,5V
Power Dissipation . . . . 1 Watt

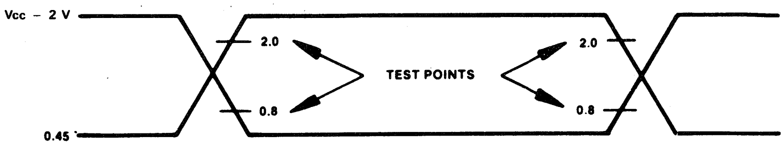
**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±10%

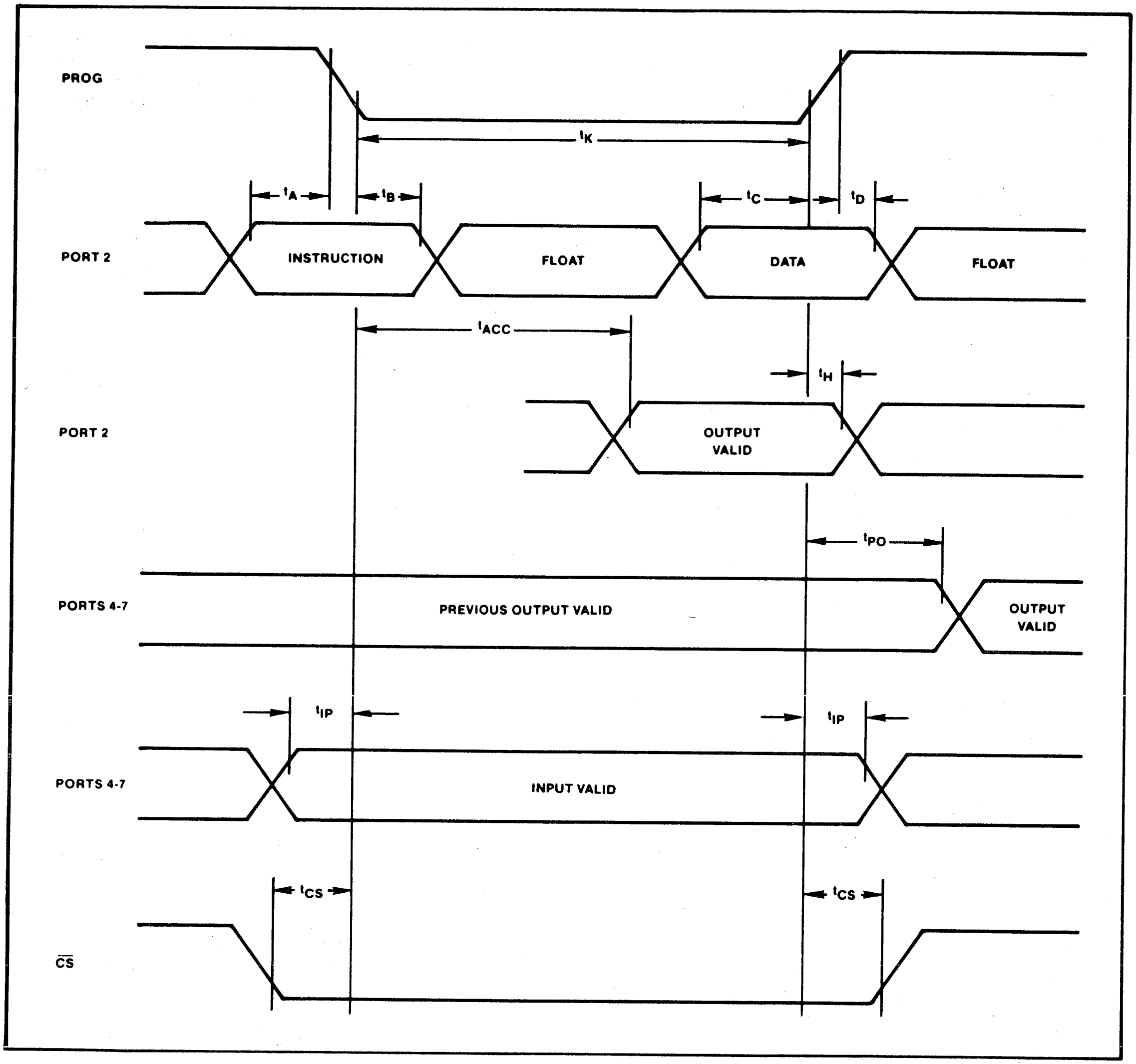
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5		0.8	V	
V_{IH}	Input High Voltage	VCC -2.0		VCC+0.5	V	
V_{OL1}	Output Low Voltage Ports 4-5			0.45	V	I_{OL} = 10 mA
V_{OL2}	Output Low Voltage Port 6-7			0.45	V	I_{OL} = 20 mA
V_{OH1}	Output High Voltage Ports 4-7	VCC -1.0			V	I_{OH} = 1.2 mA
I_{IL1}	Input Leakage Ports 4-7	-1		1	µA	V_{in} = V_{CC} to OV
I_{IL2}	Input Leakage Port 2, CS, PROG	-1		1	µA	V_{in} = V_{CC} to OV
V_{OL3}	Output Low Voltage Port 2			0.45	V	I_{OL} = 1 mA
I_{CC1}	VCC Supply Current - Operation Mode		0.7	2	mA	Write mode at 1.3 µs period TK = 700 ns all outputs opened
I_{CC2}	VCC Supply Current - Standby			10	µA	All outputs opened
V_{OH2}	Output Voltage Port 2	VCC -0.4				I_{OH} = 0.8 mA
I_{OL}	Sum of all I_{OL} from 16 Outputs			160	mA	10. mA Each Pin

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Min.	Max.	Units	Test Conditions
t_A	Code Valid Before PROG	80		ns	80 pF Load
t_B	Code Valid After PROG	50		ns	20 pF Load
t_C	Data Valid Before PROG	100		ns	80 pF Load
t_D	Data Valid After PROG	20		ns	20 pF Load
t_H	Floating After PROG	0	140	ns	20 pF Load
t_K	PROG Negative Pulse Width	700		ns	
t_{CS}	CS Valid Before/After PROG	50		ns	
t_{PO}	Ports 4-7 Valid After PROG		300	ns	100 pF Load
t_{LP1}	Ports 4-7 Valid Before/After PROG	0		ns	
t_{ACC}	Port 2 Valid After PROG		650	ns	80 pF Load



WAVEFORMS



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The maximum value for the output low current can be 30 mA for Port 6-7 but with an increase of the output low voltage V_{OL} (0.6 V)

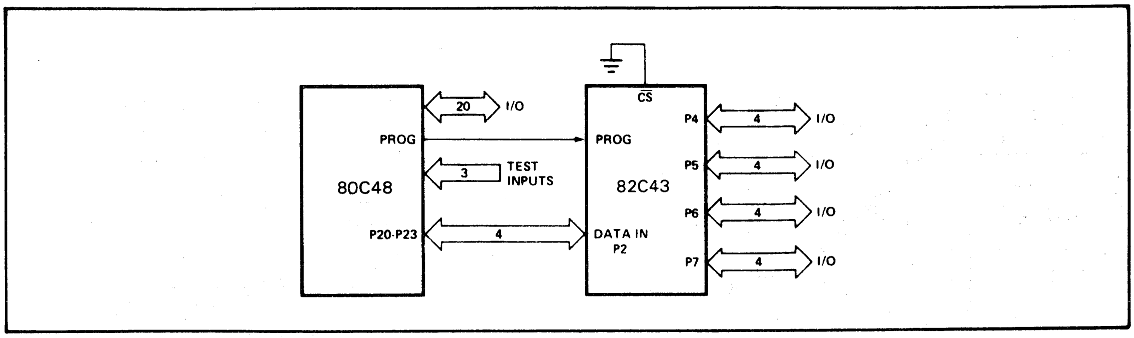

Figure 4. Expander Interface

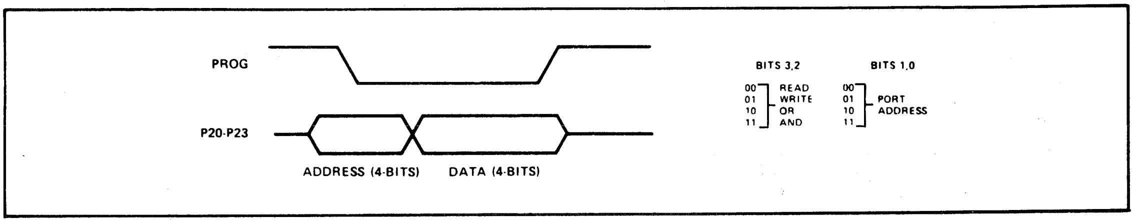

Figure 5. Output Expander Timing

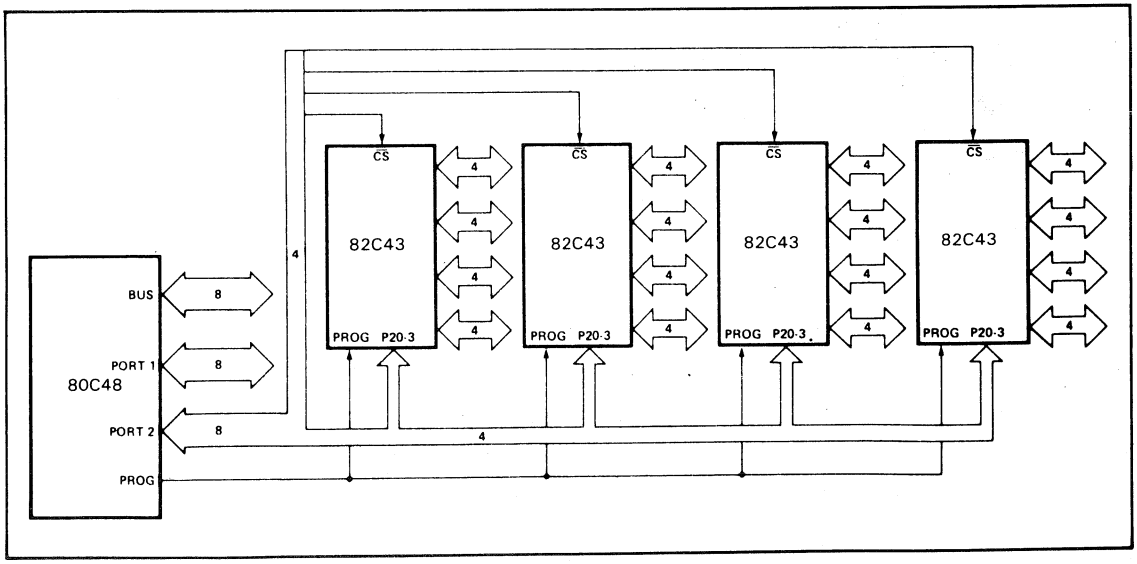

Figure 6. Using Multiple 82C43's

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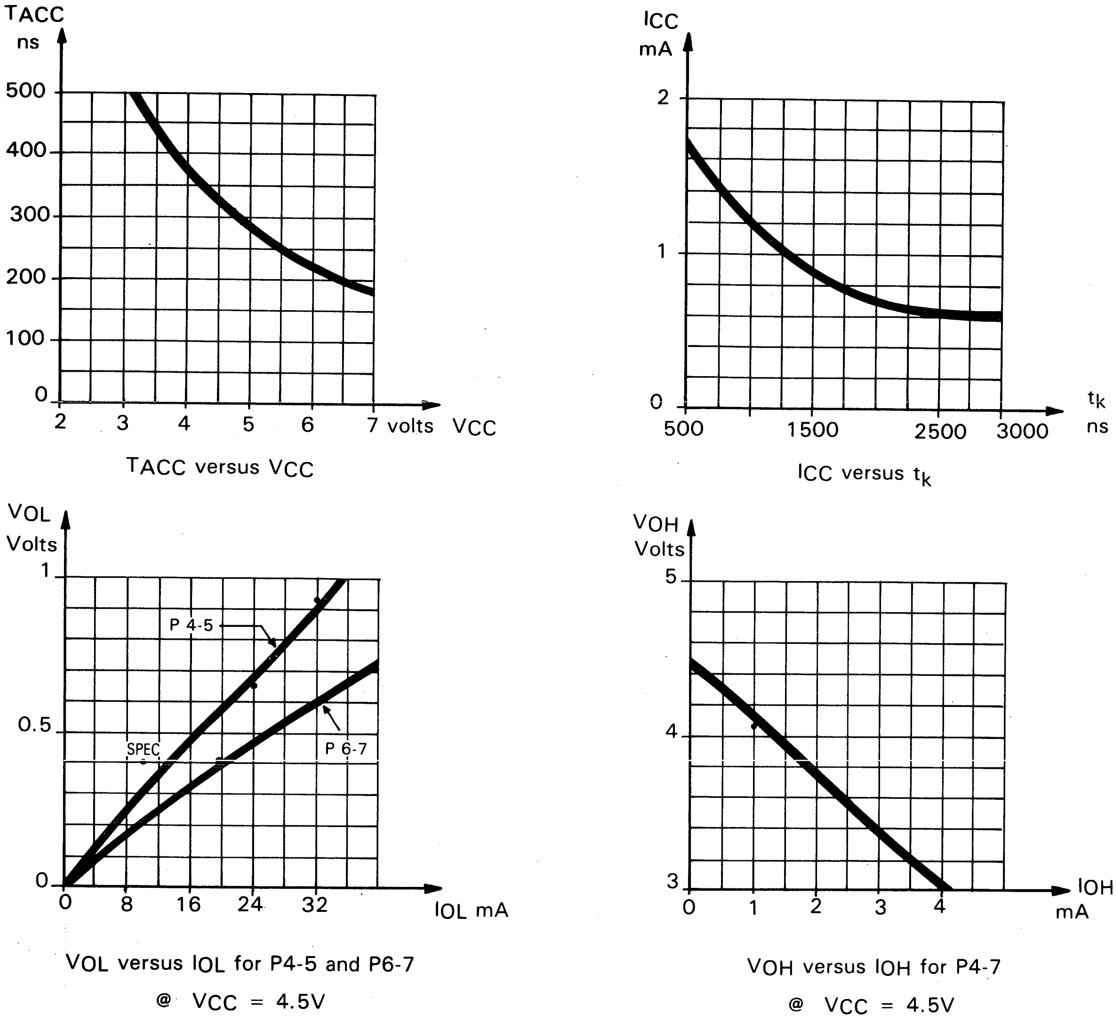

Fig. 7 : Typical evolution of key parameters

ORDERING INFORMATION		
Part N°	Package	Temperature range
D - 82C43 P - 82C43	Cerdip Plastic	Commercial 0 - 70° C

HMOS microprocessor 5

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Product information

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Product Index

ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect devices reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.

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MATRA-HARRIS SEMICONDUCTEURS

data sheet

intel

8031/8051
SINGLE-COMPONENT 8-BIT MICROCOMPUTER

PRELIMINARY

- 8031 - Control Oriented CPU With RAM and I/O
- 8051 - An 8031 With Factory Mask-Programmable ROM

- 4K x 8 ROM
- 128 x 8 RAM
- Four 8-Bit Ports, 32 I/O Lines
- Two 16-Bit Timer/Event Counters
- High-Performance Full-Duplex Serial Channel
- External Memory Expandable to 128K
- Compatible with MCS-80 /MCS-85 Peripherals
- Boolean Processor
- MCS-48 Architecture Enhanced with:
  - Non-Paged Jumps
  - Direct Addressing
  - Four 8-Register Banks
  - Stack Depth Up to 128-Bytes
  - Multiply, Divide, Subtract, Compare
- Most Instructions Execute in 1μs
- 4μs Multiply and Divide

The MHS 8031/8051 is a stand-alone, high-performance single-chip computer fabricated with Intel's highly-reliable +5 Volt, depletion-load, N-Channel, silicon-gate HMOS technology and packaged in a 40-pin DIP. It provides the hardware features, architectural enhancements and new instructions that are necessary to make it a powerful and cost effective controller for applications requiring up to 64K bytes of program memory and/or up to 64K bytes of data storage.

The 8051 contains a non-volatile 4K x 8 read-only program memory; a volatile 128 x 8 read/write data memory; 32 I/O lines; two 16-bit timer/counters; a five-source, two-priority-level, nested interrupt structure; a serial I/O port for either multi-processor communications, I/O expansion, or full duplex UART; and on-chip oscillator and clock circuits. The 8031 is identical, except that it lacks the program memory. For systems that require extra capability, the 8051 can be expanded using standard TTL compatible memories and the byte oriented MCS-80® and MCS-85® peripherals.

The 8051 microcomputer, like its 8048 predecessor, is efficient both as a controller and as an arithmetic processor. The 8051 has extensive facilities for binary and BCD arithmetic and excels in bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 15 MHz crystal, 58% of the instructions execute in 1.0μs, 40% in 2.0μs and multiply and divide require only 4.0μs. Among the many instructions added to the standard 8048 instruction set are multiply, divide, subtract and compare.

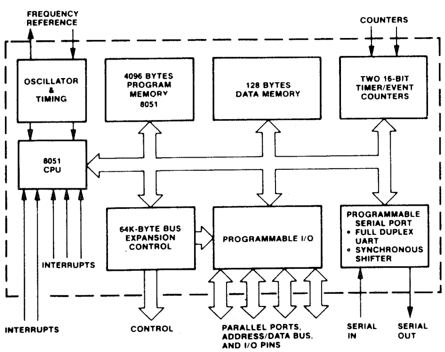

Figure 1. Block Diagram

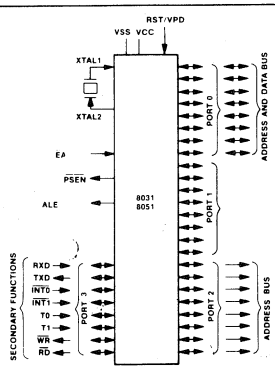

Figure 2. Logic Symbol

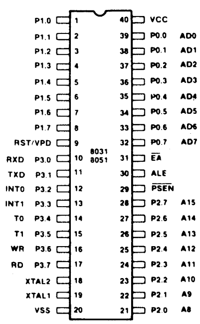

Figure 3. Pin Configuration

INTRODUCTION

This data sheet provides an introduction to the 8051 family. A detailed description of the hardware required to expand the 8051 with more program memory, data memory, I/O, specialized peripherals and into multiprocessor configurations is described in the 8051 Family User's Manual.

The 8051 Family

The 8051 is a stand-alone high-performance single-chip computer intended for use in sophisticated real-time applications such as instrumentation, industrial control and intelligent computer peripherals. It provides the hardware features, architectural enhancements and new instructions that make it a powerful and cost effective controller for applications requiring up to 64K-bytes of program memory and/or up to 64K-bytes of data storage. A Block Diagram is shown in Figure 1.

The 8031 is a control-oriented CPU without on-chip program memory. It can address 64K-bytes of external Program Memory in addition to 64K-bytes of External Data Memory. For systems requiring extra capability, each member of the 8051 family can be expanded using standard memories and the byte oriented MCS-80 and MCS-85 peripherals. The 8051 is an 8031 with the lower 4K-bytes of Program Memory filled with on-chip mask programmable ROM.

The three pin-compatible versions of this component reduce development problems to a minimum and provide maximum flexibility.

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The 8051 is well suited for low-cost, high volume production; and the 8031 for applications desiring the flexibility of external Program Memory which can be easily modified and updated in the field.

MACRO-VIEW OF THE 8051 ARCHITECTURE

On a single die the 8051 microcomputer combines CPU; non-volatile 4K x 8 read-only program memory; volatile 128 x 8 read/write data memory; 32 I/O lines; two 16-bit timer/event counters; a five-source, two-priority-level, nested interrupt structure; serial I/O port for either multi-processor communications, I/O expansion, or full duplex UART; and on-chip oscillator and clock circuits. This section will provide an overview of the 8051 by providing a high-level description of its major elements: the CPU architecture and the on-chip functions peripheral to the CPU. The generic term "8051" is used to refer collectively to the 8031 and 8051.

8051 CPU Architecture

The 8051 CPU manipulates operands in four memory spaces. These are the 64K-byte Program Memory, 64K-byte External Data Memory, 384-byte Internal Data Memory and 16-bit Program Counter spaces. The Internal Data Memory address space is further divided into the 256-byte Internal Data RAM and 128-byte Special Function Register (SFR) address spaces shown in Figure 4. Four Register Banks (each with eight registers), 128 addressable bits, and the stack reside in the Internal Data RAM. The stack depth is limited only by the available Internal Data RAM and its location is determined by the 8-bit stack pointer. All registers except the Program Counter and the four 8-Register Banks reside in the Special Function Register address space. These memory mapped registers include arithmetic registers, pointers, I/O ports, interrupt system registers, timers and serial port. 128 bit locations in the SFR address space are addressable as bits. The 8051 contains 128 bytes of Internal Data RAM and 20 SFRs.

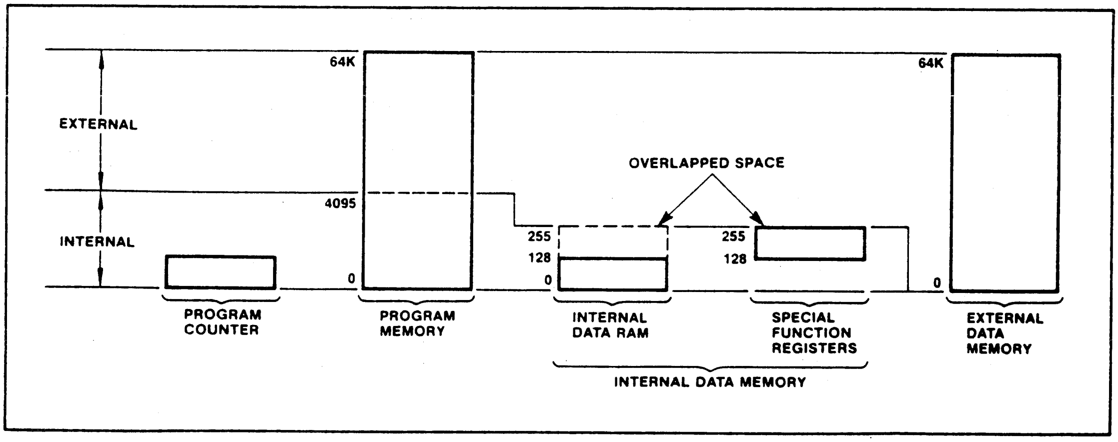

Figure 4. 8051 Family Memory Organization

The 8051 provides a non-paged Program Memory address space to accommodate relocatable code. Conditional branches are performed relative to the Program Counter. The register-indirect jump permits branching relative to a 16-bit base register with an offset provided by an 8-bit index register. Sixteen-bit jumps and calls permit branching to any location in the contiguous 64K Program Memory address space.

The 8051 has five methods for addressing source operands: Register, Direct, Register-Indirect, Immediate and Base-Register- plus Index-Register-Indirect Addressing. The first three methods can be used for addressing destination operands. Most instructions have a "destination, source" field that specifies the data type, addressing methods and operands involved. For operations other than moves, the destination operand is also a source operand.

Registers in the four 8-Register Banks can be accessed through Register, Direct, or Register-Indirect Addressing; the 128 bytes of Internal Data RAM through Direct or Register-Indirect Addressing; and the Special Function Registers through Direct Addressing. External Data Memory is accessed through Register-Indirect Addressing. Look-Up-Tables resident in Program Memory can be accessed through Base-Register- plus Index-Register- Indirect Addressing.

The 8051 is classified as an 8-bit machine since the internal ROM, RAM, Special Function Registers, Arithmetic/Logic Unit and external data bus are each 8-bits wide. The 8051 performs operations on bit, nibble, byte and double-byte data types.

The 8051 has extensive facilities for byte transfer, logic, and integer arithmetic operations. It excels at bit handling since data transfer, logic and conditional branch operations can be performed directly on Boolean variables.

The 8051's instruction set is an enhancement of the instruction set familiar to MCS-48 users. It is enhanced to allow expansion of on-chip CPU peripherals and to optimize byte efficiency and execution speed. Op codes were reassigned to add new high-power operations and to permit new addressing modes which make the old operations more orthogonal. Efficient use of program memory results from an instruction set consisting of 49 single-byte, 45 two-byte and 17 three-byte instructions. When using a 12 MHz oscillator, 64 instructions execute in 1μs and 45 instructions execute in 2μs. The remaining instructions (multiply and divide) execute in only 4μs. The number of bytes in each instruction and the number of oscillator periods required for execution are listed in the appended 8051 Instruction Set Summary.

On-Chip Peripheral Functions

Thus far only the CPU and memory spaces of the 8051 have been described. In addition to the CPU and memories, an interrupt system, extensive I/O facilities, and several peripheral functions are integrated on-chip to relieve the CPU of repetitious, complicated or time-critical tasks and to permit stringent real-time control of external system interfaces. The extensive I/O facilities include the I/O pins, parallel I/O ports, bidirectional address/data bus and the serial port for I/O expansion. The CPU peripheral functions integrated on-chip are the two 16-bit counters and the serial port. All of these work together to greatly boost system performance.

INTERRUPT SYSTEM

External events and the real-time-driven on-chip peripherals require service by the CPU asynchronous to the execution of any particular section of code. To tie the asynchronous activities of these functions to normal program execution, a sophisticated multiple-source, two-priority-level, nested interrupt system is provided. Interrupt response latency ranges from 3μs to 7μs when using a 12 MHz crystal.

The 8051 acknowledges interrupt requests from five sources: Two from external sources via the $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ pins, one from each of the two internal counters and one from the serial I/O port. Each interrupt vectors to a separate location in Program Memory for its service program. Each of the five sources can be assigned to either of two priority levels and can be independently enabled and disabled. Additionally all enabled sources can be globally disabled or enabled. Each external interrupt is programmable as either level- or transition-activated and is active-low to allow the "wire or-ing" of several interrupt sources to the input pin. The interrupt system is shown diagrammatically in Figure 5.

I/O FACILITIES

The 8051 has instructions that treat its 32 I/O lines as 32 individually addressable bits and as four parallel 8-bit ports addressable as Ports 0, 1, 2 and 3. Ports 0, 2 and 3 can also assume other functions. Port 0 provides the multiplexed low-order address and data bus used for expanding the 8051 with standard memories and peripherals. Port 2 provides the high-order address bus when expanding the 8051 with external Program Memory or more than 256 bytes of External Data Memory. The pins of Port 3 can be configured individually to provide external interrupt request inputs, counter inputs, the serial port's receiver input and transmitter output, and to generate the control signals used for reading and writing External Data Memory. The generation or use of a secondary function on a Port 3 pin is done automatically by the 8051 as long as the pin

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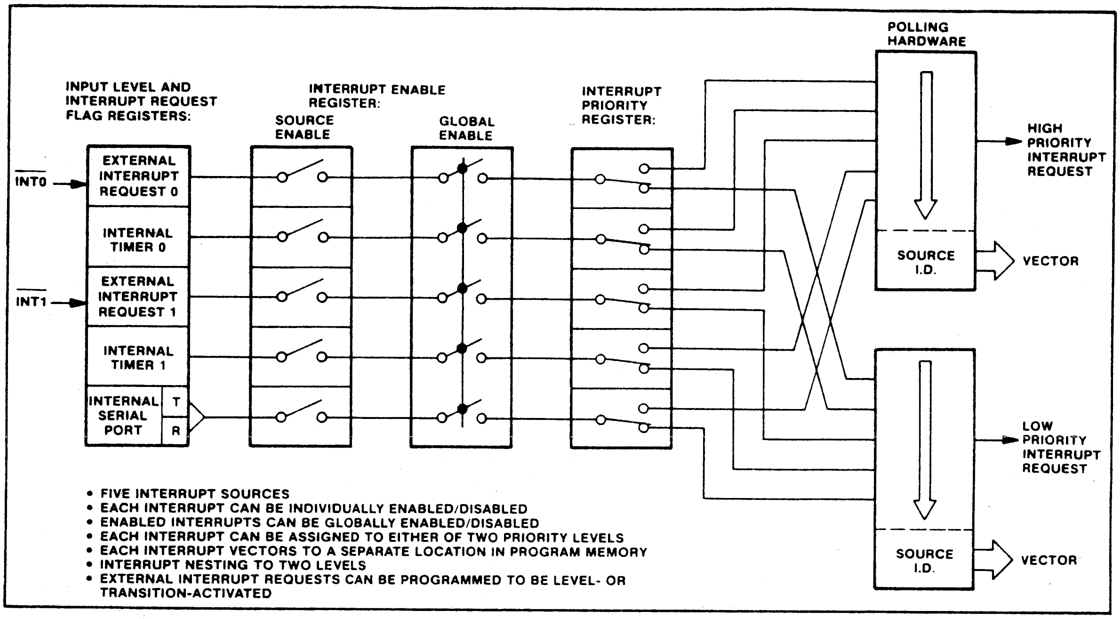

Figure 5. 8051 Interrupt System

is configured as an input. The configuration of the ports is shown on the 8051 Family Logic Symbol of Figure 2.

Open Drain I/O Pins

Each pin of Port 0 can be configured as an open drain output or as a high impedance input. Resetting the microcomputer programs each pin as an input by writing a one (1) to the pin. If a zero (0) is later written to the pin it becomes configured as an output and will continuously sink current. Re-writing the pin to a one (1) will place its output driver in a high-impedance state and configure the pin as an input. Each I/O pin of Port 0 can sink two TTL loads.

Quasi-Bidirectional I/O Pins

Ports 1, 2 and 3 are quasi-bidirectional buffers. Each quasi-bidirectional buffer has an internal pullup resistor of approximately 20K- to 40K-ohms connected between its I/O pin and the positive power supply pin. Resetting the microcomputer programs each pin as an input by writing a one (1) to the pin. If a zero (0) is later written to the pin it becomes configured as an output and will continuously sink current. Any pin that is configured as an output will be reconfigured as an input when a one (1) is written to the pin. Simultaneous to this reconfiguration, the output driver in the quasi-bidirectional buffer will source current for two oscillator periods. Since the output driver sources current only when a bit previously written to a zero (0) is updated to a one (1), a pin programmed as an input will not source a current spike into the TTL gate that is driving it if the pin is later written with another one (1). Since the output driver in the quasi-bidirectional buffer sources current for only two oscillator periods, the internal pullup resistor is provided to hold the external driver's loading at a TTL high level. Ports 1, 2 and 3 can sink/source one TTL load.

Microprocessor Bus

A microprocessor bus is provided to permit the 8051 to solve a wide range of problems and to allow the upward growth of user products. This multiplexed address and data bus provides an interface compatible with standard memories, MCS-80 peripherals and the MCS-85 memories that include on-chip programmable I/O ports and timing functions. These are summarized in the 8051 Microcomputer Expansion Components chart of Figure 6.

When accessing external memory the high-order address is emitted on Port 2 and the low-order address on Port 0. The ALE signal is provided for strobing the address into an external latch. The program store enable ($\overline{\text{PSEN}}$) signal is provided for enabling an external memory device to Port 0 during a read from the Program Memory address space. When the MOVX instruction is executed Port 3 automatically generates the read ($\overline{\text{RD}}$) signal for enabling an External Data Memory device to Port 0 or generates the write ($\overline{\text{WR}}$) signal for strobing the external memory device with the data emitted by Port 0. Port 0 emits the address and data to the external memory through a push/pull driver that can sink/source two TTL loads. At the end of the read/write bus cycle Port 0 is automatically reprogrammed to its high

	Category	I.D.	Description	Comments	Program Or Data Memory	Crystal Frequency MHz (Max)
	I/O Expander		8 Line I/O Expander (Shift Register)	Low Cost I/O Expander		12
Compatible MCS-80/85 Components	Standard EPROMs	2758 2716-1 2732 2732A	1K x 8 450 ns Light Erasable 2K x 8 350 ns Light Erasable 4K x 8 450 ns Light Erasable 4K x 8 250 ns Light Erasable	User programmable and erasable.	P P P P	9 11 9 12
	Standard RAMs	2114A 2148 2142-2	1K x 4 100 ns RAM 1K x 4 70 ns RAM 1K x 4 200 ns RAM	Data memory can be easily expanded using standard NMOS RAMs.	D D D	12 12 12
	Multiplexed Address/ Data RAMs	8185A	1K x 8 300 ns RAM		D	12
	Standard I/O	8212 8282 8283 8255A 8251A	8-Bit I/O Port 8-Bit I/O Port 8-Bit I/O Port Programmable Peripheral Interface Programmable Communications Interface	Serves as Address Latch or I/O port. Three 8-bit programmable I/O ports. Serial Communications Receiver/Transmitter.	D D D D D	12 12 12 12 12
	Standard Peripherals	8205 8286 8287 8253A 8279 8291 8292	1 of 8 Binary Decoder Bi-directional Bus Driver Bi-directional Bus Driver (Inverting) Programmable Interval Timer Programmable Keyboard/Display Interface (128 Keys) GPIB Talker/Listener GPIB Controller	MCS-80 and MCS-85 peripheral devices are compatible with the 8051 allowing easy addition of specialized interfaces. Future MCS-80/85 devices will also be compatible.	D D D D D D D	12 12 12 12 12 12 11.7
	Universal Peripheral Interfaces	8041A 8741A	ROM Program Memory EPROM Program Memory	User programmable to perform custom I/O and control functions.	D/P D/P	12/11.7 12/11.7
	Memories with on-chip I/O and Peripheral Functions.	8155-2 8355-2 8755-2	256 x 8 330 ns RAM 2K x 8 330 ns ROM 2K x 8 330 ns EPROM		D P P	12 11.6 11.6

Figure 6. 8051 Microcomputer Expansion Components

impedance state and Port 2 is returned to the state it had prior to the bus cycle. The 8051 generates the address, data and control signals needed by memory and I/O devices in a manner that minimizes the requirements placed on external program and data memories. At 12 MHz, the Program Memory cycle time is 500ns and the access times required from stable address and $\overline{\text{PSEN}}$ are approximately 320ns and 150ns respectively. The External Data Memory cycle time is 1μs and the access times required from stable address and from read ($\overline{\text{RD}}$) or write ($\overline{\text{WR}}$) command are approximately 600ns and 250ns respectively.

TIMER/EVENT COUNTERS

The 8051 contains two 16-bit counters for measuring time intervals, measuring pulse widths, counting events and generating precise, periodic interrupt requests. Each can be programmed independently to operate similar to an 8048 8-bit timer with divide by 32 prescaler or as an 8-bit counter with divide by 32 prescaler (Mode 0), as a 16-bit time-interval or event counter (Mode 1), or as an 8-bit time-interval or event counter with automatic reload upon overflow (Mode 2).

Additionally, counter 0 can be programmed to a mode that divides it into one 8-bit time-interval or event counter and one 8-bit time-interval counter (Mode 3). When counter 0 is in Mode 3, counter 1 can be programmed to any of the three aforementioned modes, although it cannot set an interrupt request flag or generate an interrupt. This mode is useful because counter 1's overflow can be used to pulse the serial port's transmission-rate generator. Along with their multiple operating modes and 16-bit precision, the counters can also handle very high input frequencies. These range from 0.1 MHz to 1.0 MHz (for 1.2 MHz to 12 MHz crystal) when programmed for an input that is a division by 12 of the oscillator frequency and from 0 Hz to an upper limit of 50 KHz to 0.5 MHz (for 1.2 MHz to 12 MHz crystal) when programmed for external inputs. Both internal and external inputs can be gated to the counter by a second external source for directly measuring pulse widths.

The counters are started and stopped under software control. Each counter sets its interrupt request flag when it overflows from all ones to all zeros (or auto-reload value). The operating modes and input sources are summarized in Figures 7 and 8. The effects of the configuration flags and the status flags are shown in Figures 9 and 10.

SERIAL COMMUNICATIONS

The 8051 has a serial I/O port that is useful for serially linking peripheral devices as well as multiple 8051s through standard asynchronous protocols with full-duplex operation. The serial port also has a synchronous mode for expansion of I/O lines using CMOS and TTL shift registers. This hardware serial communications interface saves ROM code and permits a much higher transmission rate than could be achieved through software. In response to a serial port interrupt request the CPU has only to read/write the serial port's buffer to service the serial link. A block diagram of the serial port is shown in Figures 11 and 12. Methods for linking UART (universal asynchronous receiver/transmitter) devices are

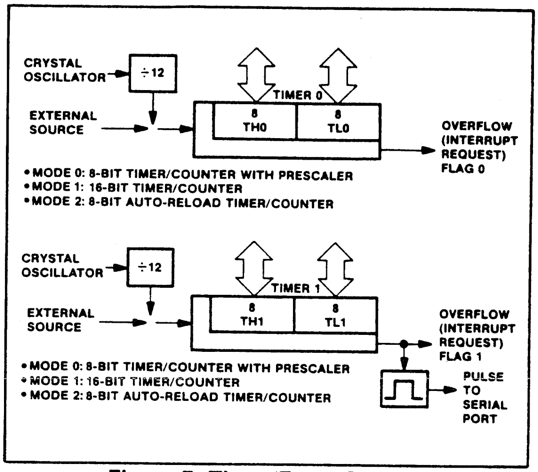

Figure 7. Timer/Event Counter Modes 0, 1 and 2

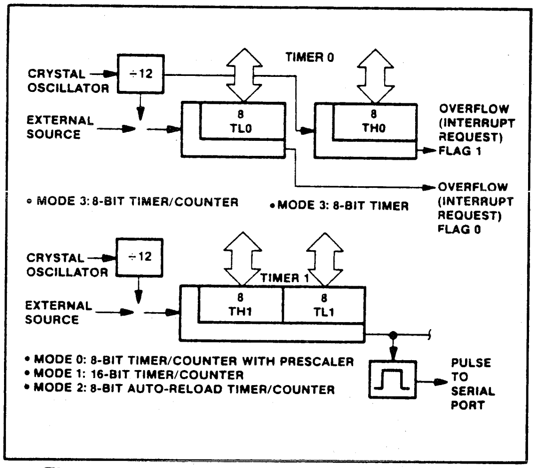

Figure 8. Timer/Event Counter 0 in Mode 3

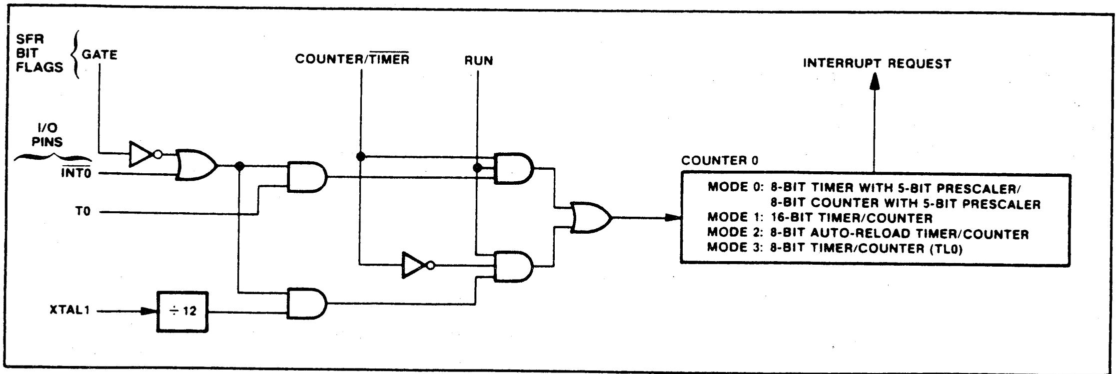

Figure 9. Timer/Counter 0 Control and Status Flag Circuitry

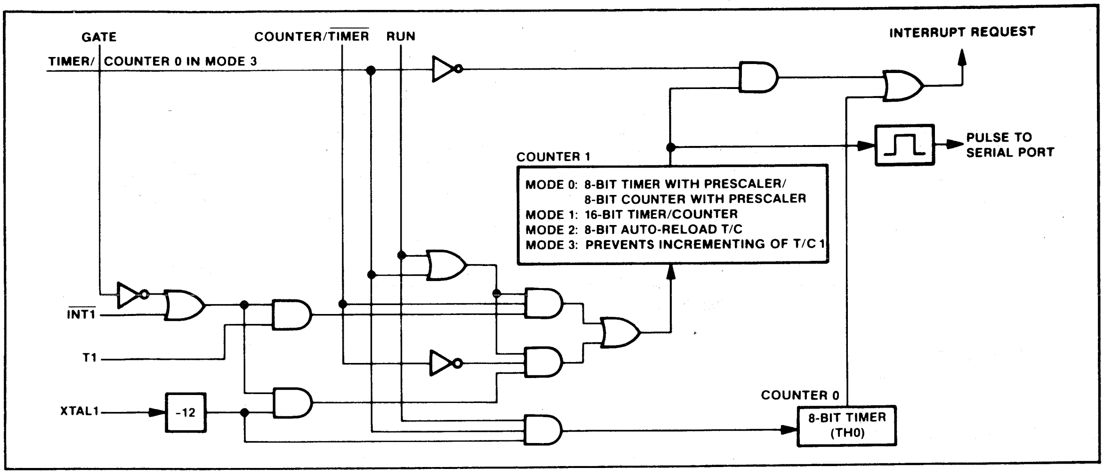

Figure 10. Timer/Counter 1 Control and Status Flag Circuitry

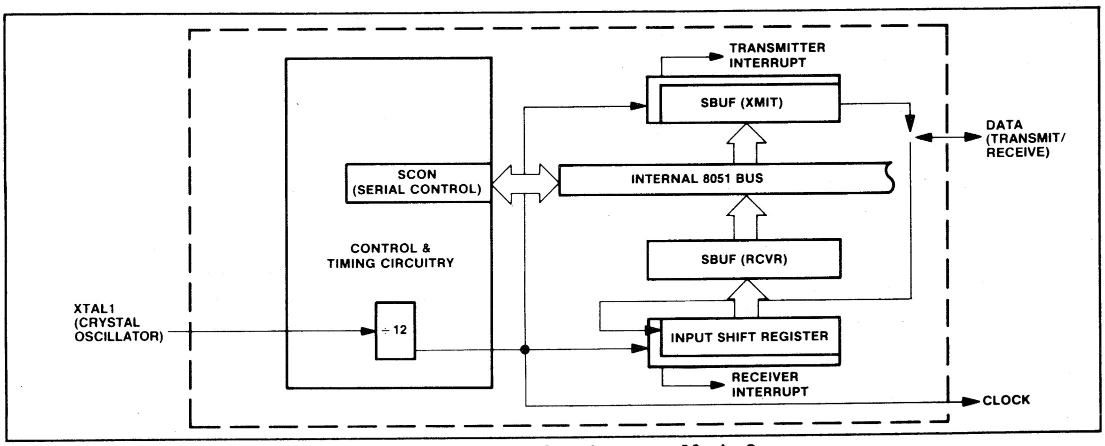

Figure 11. Serial Port—Synchronous Mode 0

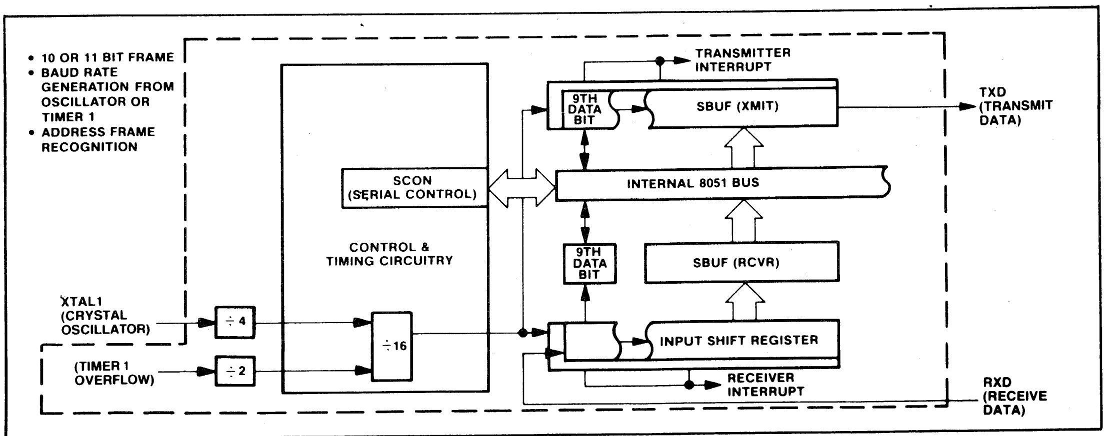

Figure 12. Serial Port—UART Modes 1, 2, and 3

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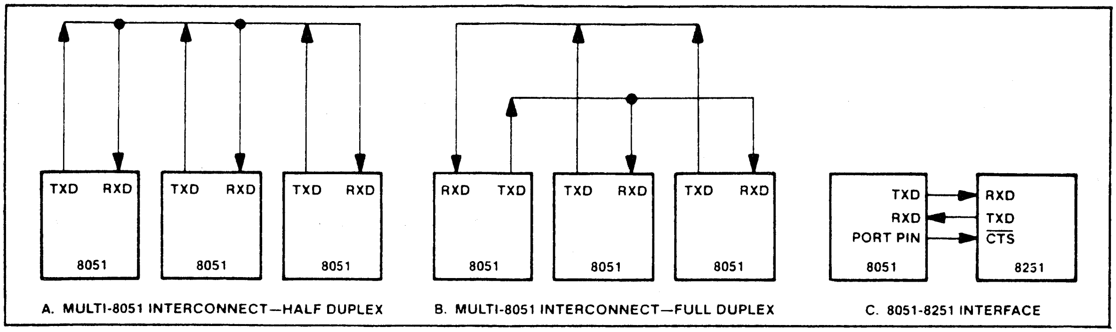

Figure 13. UART Interfacing Schemes

shown in Figure 13 and a method for I/O expansion is shown in Figure 14.

The full-duplex serial I/O port provides asynchronous modes to facilitate communications with standard UART devices, such as printers and CRT terminals, or communications with other 8051s in multi-processor systems. The receiver is double buffered to eliminate the overrun that would occur if the CPU failed to respond to the receiver's interrupt before the beginning of the next frame. Double buffering of the transmitter is not needed since the 8051 can generally maintain the serial link at its maximum rate without it. A minor degradation in transmission rate can occur in rare events such as when the servicing of the transmitter has to wait for a lengthy interrupt service program to complete. In asynchronous modes, false start-bit rejection is provided on received frames. For noise rejection a best two-out-of-three vote is taken on three samples near the center of each received bit.

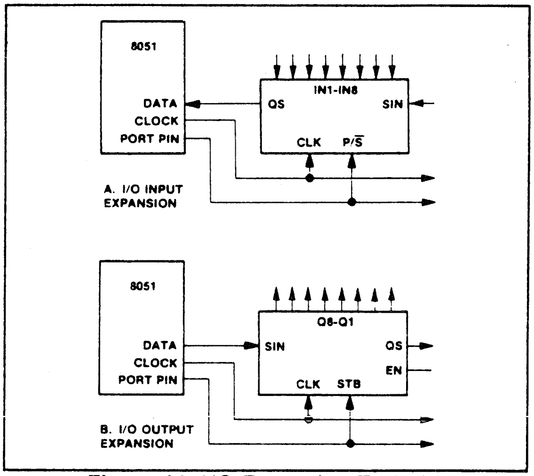

Figure 14. I/O Expansion Technique

When interfacing with standard UART devices the serial channel can be programmed to a mode (Mode 1) that transmits/receives a ten-bit frame or programmed to a mode (Mode 2 or 3) that transmits/ receives an eleven-bit frame as shown in Figure 15. The frame consists of a start bit, eight or nine data bits and a stop bit. In Modes 1 and 3, the transmission-rate timing circuitry receives a pulse from counter 1 each time the counter overflows. The input to counter 1 can be an external source or a division by 12 of the oscillator frequency. The auto-reload mode of the counter provides communication rates of 122 to 31,250 bits per second (including start and stop bits) for a 12 MHz crystal In Mode 2 the communication rate is a division by 64 of the oscillator frequency yielding a transmission rate of 187,500 bits per second (including start and stop bits) for a 12 MHz crystal.

Distributed processing offers a faster, more powerful system than can be provided by a single CPU processor. This results from a hierarchy of interconnected processors, each with its own memories and

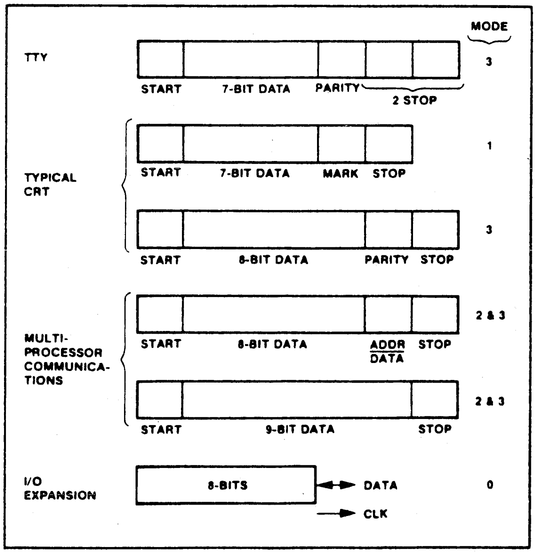

Figure 15. Typical Frame Formats

1. Slaves—Configure serial port to interrupt CPU if the received ninth data bit is a one (1).
2. Master—Transmit frame containing address in first 8 data bits and set ninth data bit (i.e. ninth data bit designates address frame).
3. Slaves—Serial port interrupts CPU when address frame is received. Interrupt service program compares received address to its address. The slave which has been addressed reconfigures its serial port to interrupt the CPU on all subsequent transmissions.
4. Master—Transmit control frames and data frames (these will be accepted only by the previously addressed slave).

Figure 16. Protocol for Multi-Processor Communications

I/O. In multiprocessing, a host 8051 microcomputer controls a multiplicity of 8051s configured to operate simultaneously on separate portions of the program, each controlling a portion of the overall process. The interconnected 8051s reduce the load on the host processor and result in a low-cost system of data transmission. This form of distributed processing is especially effective in systems where controls in a complex process are required at physically separated locations.

In Modes 2 and 3 the automatic wake-up of slave processors through interrupt driven address-frame recognition is provided to facilitate interprocessor communications. The protocol for interprocessor communications is shown in Figure 16.

In synchronous mode (Mode 0) the high speed serial port provides an efficient, low-cost method of expanding I/O lines using standard TTL and CMOS shift registers. The serial channel provides a clock output for synchronizing the shifting of bits to/from an external register. The data rate is a division by 12 of the oscillator frequency and is 1M bits per second at 12 MHz.

8051 FAMILY PIN DESCRIPTION

VSS

Circuit ground potential.

VCC

+5V power supply during operation and program verification.

PORT 0

Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source eight LS TTL loads.

PORT 1

Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. Port 1 can sink/source three LS TTL loads.

PORT 2

Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source three LS TTL loads.

PORT 3

Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and $\overline{RD}$ and $\overline{WR}$ pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source three LS TTL loads. The secondary functions are assigned to the pins of Port 3, as follows:

—RXD/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous).
—TXD/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous).
—$\overline{INT0}$ (P3.2). Interrupt 0 input or gate control input for counter 0.
—$\overline{INT1}$ (P3.3). Interrupt 1 input or gate control input for counter 1.
—T0 (P3.4). Input to counter 0.
—T1 (P3.5). Input to counter 1.
—$\overline{WR}$ (P3.6). The write control signal latches the data byte from Port 0 into the External Data Memory.
—$\overline{RD}$ (P3.7). The read control signal enables External Data Memory to Port 0.

RST/VPD

A high level on this pin resets the 8051. A small internal pulldown resistor permits power-on reset using only a capacitor connected to VCC. If VPD is held within its spec while VCC drops below spec, VPD will provide standby power to the RAM. When VPD is low, the RAM's current is drawn from VCC.

ALE

Provides Address Latch Enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.

$\overline{PSEN}$

The Program Store Enable output is a control signal that enables the external Program Memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.

$\overline{EA}$
When held at a TTL high level, the 8051 executes instructions from the internal ROM when the PC is less than 4096. When held at a TTL low level, the 8051 fetches all instructions from external Program Memory.

XTAL 1
Input to the oscillator's high gain amplifier. Required when a crystal is used. Connect to VSS when external source is used on XTAL 2.

XTAL 2
Output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.

8051 FAMILY DEVELOPMENT SYSTEM AND SOFTWARE SUPPORT

The 8051 is supported by a total range of Intel development tools. This broad range of support shortens the product development cycle and thus brings the product to market sooner.

- ASM51 Absolute macro assembler for the 8051.
- CONV51 8048 assembly language source code to 8051 assembly source code conversion program.
- EM-51 8051 emulator board that uses a modified 8051 and an EPROM.
- ICE-51™ Real-time in-circuit emulator.
- SDK-51 System design kit for developing user Prototype around the 8051.
- 8051 Workshop.

5

8051 Software Development Package (ASM51 and CONV51)

The 8051 software development package provides development system support for the powerful 8051 family of single-chip microcomputers. The package contains a symbolic macro assembler and a 8048 to 8051 source code converter. This diskette-based software package runs under ISIS-II on any Intellec® Microcomputer Development System with 64K bytes of memory.

8051 Macro Assembler (ASM51)

The 8051 macro assembler translates symbolic 8051 assembly language instructions into machine executable object code. These assembly language mnemonics are easier to program and are more readable than binary or hexidecimal machine instructions. Also, by allowing the programmer to give symbolic names to memory locations rather than absolute addresses, software design and debug are performed more quickly and reliably.

ASM51 provides symbolic access for the many useful addressing methods in the 8051 architecture which reference bit, nibble and byte locations. The assembler supports macro definitions and calls. This provides a convenient means of programming a frequently used code sequence only once. The assembler also provides conditional assembly capabilities. Cross referencing is provided in the symbol table listing, which shows the user the lines in which each symbol was defined and referenced.

The object code generated is sent to MHS for fabricating the 8051 ROM version. The assembler output can also be debugged using the ICE-51 in-circuit emulator.

8048 to 8051 Assembly Language Converter Utility Program (CONV51)

The 8048 to 8051 assembly language converter is a utility to help users of the MCS-48 family of microcomputers upgrade their designs to the high performance 8051 architecture. By converting 8048 source code to 8051 source code, the investment in software developed for the 8048 is maintained when the system is upgraded.

8051 Emulation Board (EM-51)

The EM-51 8051 emulation board is a small (2.85" x 5.25") board which emulates an 8031/8051 microcomputer using standard PROMs or EPROMs in place of the 8051's on-chip program memory. The board includes a modified 8051 microcomputer, supporting circuits, and two sockets for program memory. The user may select two 2716 EPROMs, a 2732 EPROM, or two 3636 bipolar PROMs depending on crystal frequency and power requirements.

8051 In-Circuit Emulator (ICE-51™)

The 8051 In-Circuit Emulator resides in the Intellec development system. The development system interfaces with the user's 8051 system through an in-cable buffer box with the cable terminating in an 8051 pin-compatible plug. Together these replace the 8051 device in the system. With the emulator plug in place, the designer can exercise the system in real-time while collecting up to 255 instruction cycles of real-time data. In addition, he can single step the system program.

Static RAM memory is available in the ICE-51 buffer box to emulate the 8051's internal and external program memories and external data memory. The designer can display and alter the contents of the replacement memory in the ICE-51 buffer box, internal 8051 registers, internal data RAM, and Special Function Registers. Symbolic reference capability allows the designer to use meaningful symbols provided by ASM51 rather than absolute values when examining and modifying these memory, register, flag, and I/O locations in his system.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . 0 to 70°C
Storage Temperature . . . . -65°C to +150°C
Voltage on Any Pin With
  Respect to Ground (Vss) . . . . -0.5V to +7V
Power Dissipation . . . . 2 Watts

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliabilty.*

DC CHARACTERISTICS (TA = 0C to 70C; VCC = 4.75V to 5.25V; VSS =0V)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
VIL	Input Low Voltage	-0.5		0.8	V	
VIH	Input High Voltage (Except RST/VPD and XTAL2)	2.0		VCC+0.5	V	
VIH1	Input High Voltage To RST/VPD For Reset, XTAL2	2.5			V	XTAL1 to VSS
VPD	Power Down Voltage To RST/VPD	4.5		5.5	V	VCC =0V
VOL	Output Low Voltage Ports 1, 2, 3 (Note 1)			0.45	V	IOL = 1.6mA
VOL1	Output Low Voltage Port 0, ALE, /PSEN (Note 1)			0.45	V	IOL = 3.2mA
VOH	Output High Voltage Ports 1, 2, 3	2.4			V	IOH = -60μA
VOH1	Output High Voltage Port 0, ALE, /PSEN	2.4			V	IOH = -400μA
IIL	Logical 0 Input Current XTAL2, Ports 1, 2, 3			-800	μA	XTAL1 at VSS VIL = 0.45V
IIH1	Input High Current To RST/VPD For Reset			500	μA	Vin = VCC—1.5V
ILI	Input Leakage Current To Port 0, /EA			10	μA	0 < Vin < VCC
ICC	Power Supply Current		125	160	mA	
IPD	Power Down Current		10	20	mA	
CIO	Capacitance of I/O Buffer			10	pF	fc = 1MHz

Note 1: VOL is degraded when the 8051 rapidly discharges external capacitance. This A.C. noise is most pronounced during emission of address data. When using external memory, locate the latch or buffer as close to the 8051 as possible.

Datum	Emitting Ports	Time Interval	Degraded I/O Lines	VOL (peak) (max)
Address	P2, P0	T3, T9	P1, P3	.8V
Write Data	P0	T6	P1, P3, ALE	.8V

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A.C. CHARACTERISTICS (T_A 0° C to 70° C; V_{CC} = 5V ± 5%; V_{SS} = 0V; C_L for Port 0, ALE and $\overline{PSEN}$ Outputs = 100 pF; C_L for All Other Outputs = 80 pF)

Program Memory Characteristics

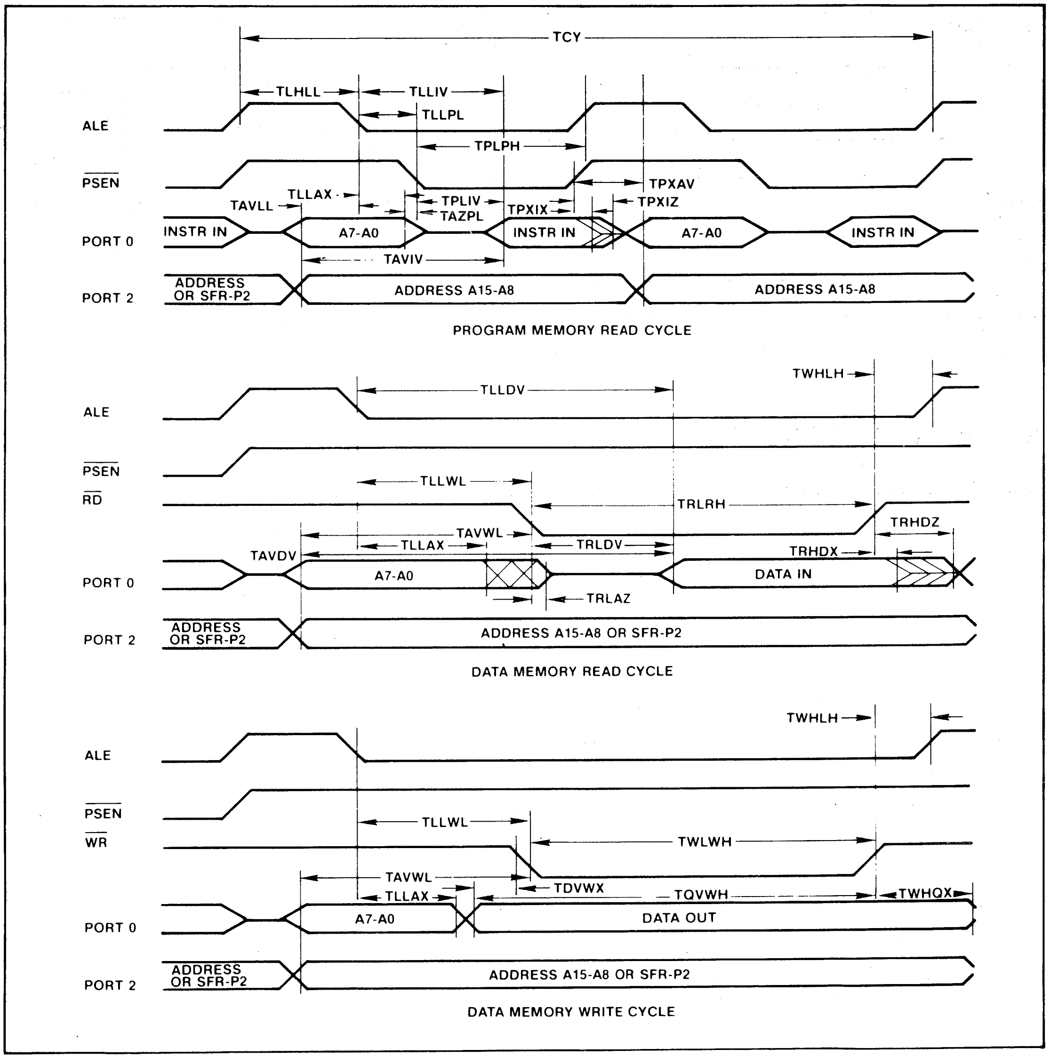
Symbol	Parameter	12 MHz Clock			Variable Clock 1/TCLCL = 1.2 MHz to 12 MHz		
		Min	Max	Units	Min	Max	Units
TLHLL	ALE Pulse Width	127		ns	2TCLCL-40		ns
TAVLL	Address Setup to ALE	53		ns	TCLCL-30		ns
TLLAX	Address Hold After ALE	48		ns	TCLCL-35		ns
TLLIV	ALE To Valid Instr In		233	ns		4TCLCL-100	ns
TLLPL	ALE To $\overline{PSEN}$	58		ns	TCLCL-25		ns
TPLPH	$\overline{PSEN}$ Pulse Width	215		ns	3TCLCL-35		ns
TPLIV	$\overline{PSEN}$ To Valid Instr In		150	ns		3TCLCL-100	ns
TPXIX	Input Instr Hold After $\overline{PSEN}$	0		ns	0		ns
*TPXIZ	Input Instr Float After $\overline{PSEN}$		63	ns		TCLCL-20	ns
*TPXAV	Address Valid After $\overline{PSEN}$	75		ns	TCLCL-8		ns
TAVIV	Address To Valid Instr In		302	ns		5TCLCL-115	ns
TAZPL	Address Float To $\overline{PSEN}$	0		ns	0		ns

***NOTE 1:** Interfacing the 8051 to devices with float times up to 75ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers.

External Data Memory Characteristics

Symbol	Parameter	12 MHz Clock			Variable Clock 1/TCLCL = 1.2 MHz to 12 MHz		
		Min	Max	Units	Min	Max	Units
TRLRH	$\overline{RD}$ Pulse Width	400		ns	6TCLCL-100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		ns	6TCLCL-100		ns
TLLAX	Address Hold After ALE	48		ns	TCLCL-35		
TRLDV	$\overline{RD}$ To Valid Data In		250	ns		5TCLCL-165	ns
TRHDX	Data Hold After $\overline{RD}$	0		ns	0		ns
TRHDZ	Data Float After $\overline{RD}$		97	ns		2TCLCL-70	ns
TLLDV	ALE To Valid Data In		517	ns		8TCLCL-150	ns
TAVDV	Address To Valid Data In		585	ns		9TCLCL-165	ns
TLLWL	ALE To $\overline{WR}$ or $\overline{RD}$	200	300	ns	3TCLCL-50	3TCLCL+50	ns
TAVWL	Address To $\overline{WR}$ or $\overline{RD}$	203		ns	4TCLCL-130		ns
TWHLH	$\overline{WR}$ or $\overline{RD}$ High To ALE High	43	123	ns	TCLCL-40	TCLCL+40	ns
TDVWX	Data Valid To $\overline{WR}$ Transition	33		ns	TCLCL-50		ns
TQVWH	Data Setup Before $\overline{WR}$	433		ns	7TCLCL-150		ns
TWHQX	Data Hold After $\overline{WR}$	33		ns	TCLCL-50		ns
TRLAZ	Address Float After $\overline{RD}$		0	ns		0	ns

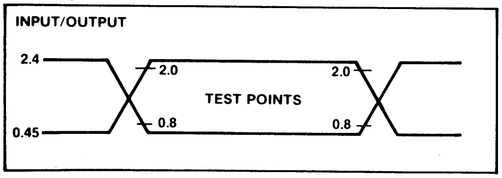
WAVEFORMS

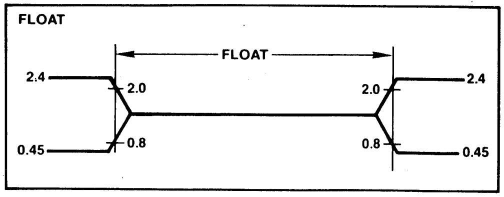


TCY
TLHLL
TLLIV
TLLPL
TPLPH
ALE
PSEN
TPXAV
TAVLL
TLLAX
TPLIV
TPXIX
TPXIZ
TAZPL
INSTR IN
A7-A0
INSTR IN
A7-A0
INSTR IN
PORT 0
TAVIV
ADDRESS OR SFR-P2
ADDRESS A15-A8
ADDRESS A15-A8
PORT 2
PROGRAM MEMORY READ CYCLE
TWHLH
TLLDV
ALE
PSEN
TLLWL
RD
TRLRH
TRHDZ
TAVWL
TLLAX
TRLDV
TAVDV
TRHDX
A7-A0
DATA IN
PORT 0
TRLAZ
ADDRESS OR SFR-P2
ADDRESS A15-A8 OR SFR-P2
PORT 2
DATA MEMORY READ CYCLE
TWHLH
ALE
PSEN
TLLWL
WR
TWLWH
TAVWL
TDVWX
TLLAX
TQVWH
TWHQX
A7-A0
DATA OUT
PORT 0
ADDRESS OR SFR-P2
ADDRESS A15-A8 OR SFR-P2
PORT 2
DATA MEMORY WRITE CYCLE

5

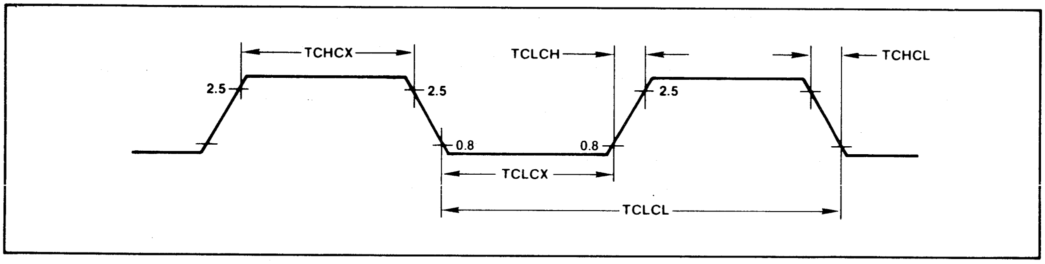
AC TESTING INPUT, OUTPUT, FLOAT WAVEFORMS





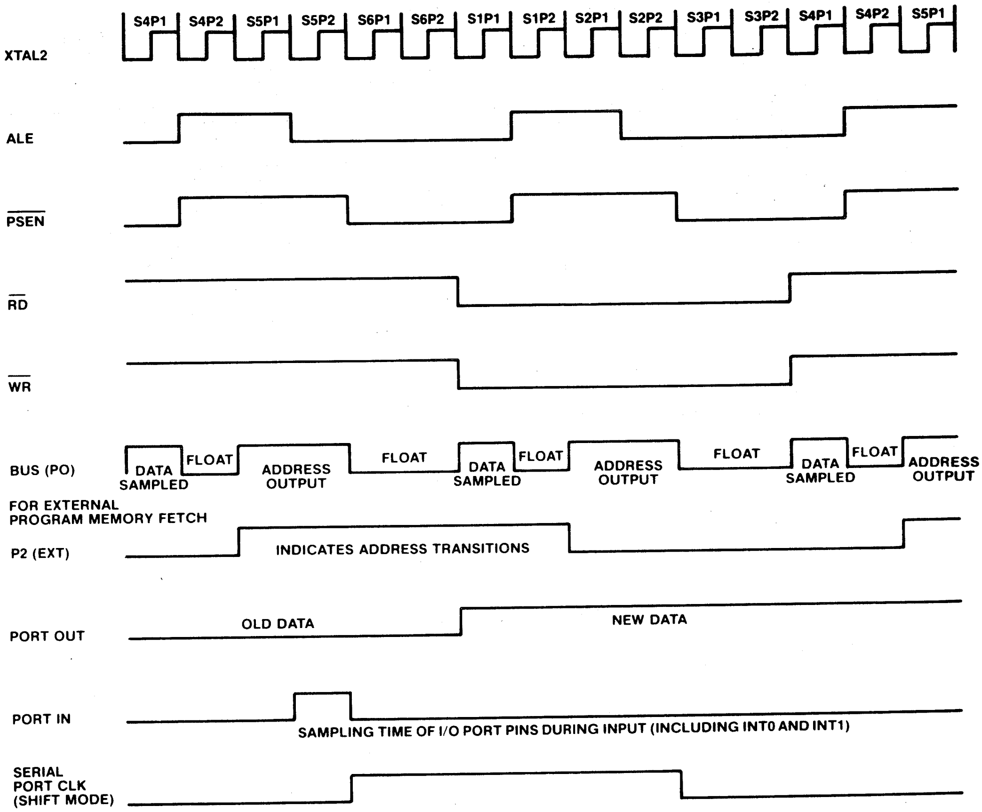
AC testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".
Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".
For timing purposes, the float state is defined as the point at which a P0 pin sinks 3.2mA or sources 400 μA at the voltage test levels.

EXTERNAL CLOCK DRIVE XTAL2



Symbol	Parameter	Variable Clock Freq = 1.2 MHz to 12 MHz Min	Max	Unit
TCLCL	Oscillator Period	83.3	833.3	ns
TCHCX	High Time	20	TCLCL-TCLCX	ns
TCLCX	Low Time	20	TCLCL-TCHCX	ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

WAVEFORM



ALL INTERNAL TIMING IS REFERENCED TO THE INTERNAL TIME STATES SHOWN AT THE TOP OF THE PAGE THIS WAVEFORM REPRESENTS THE SIGNAL ON THE X2 INPUT OF THE OSCILLATOR THIS DIAGRAM REPRESENTS WHEN THESE SIGNALS ARE ACTUALLY CLOCKED WITHIN THE CHIP HOWEVER, THE TIME IT TAKES A SIGNAL TO PROPAGATE TO THE PINS IS IN THE RANGE OF 50-150ns. PROP DELAYS ARE DEPENDENT ON MANY VARIABLES, SUCH AS TEMPERATURE, PIN LOADING, EVEN THE DIFFERENT SIGNALS VARY TYPICALLY THOUGH, /RD AND /WR HAVE PROP DELAYS OF APPROXIMATELY 50ns AND THE OTHER TIMING SIGNALS APPROXIMATELY 85ns. AT ROOM TEMPERATURE, FULLY LOADED. THESE DIFFERENCES IN PROP DELAYS BETWEEN SIGNALS HAVE BEEN INTEGRATED INTO THE TIMING SPECS

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Table 1. MCS®-51 Instruction Set Description

ARITHMETIC OPERATIONS

Mnemonic		Description	Byte	Cyc
ADD	A,Rn	Add register to Accumulator	1	1
ADD	A,direct	Add direct byte to Accumulator	2	1
ADD	A,@Ri	Add indirect RAM to Accumulator	1	1
ADD	A,#data	Add immediate data to Accumulator	2	1
ADDC	A,Rn	Add register to Accumulator with Carry	1	1
ADDC	A,direct	Add direct byte to A with Carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with Carry flag	1	1
ADDC	A,#data	Add immediate data to A with Carry flag	2	1
SUBB	A,Rn	Subtract register from A with Borrow	1	1
SUBB	A,direct	Subtract direct byte from A with Borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A w Borrow	1	1
SUBB	A,#data	Subtract immed. data from A w Borrow	2	1
INC	A	Increment Accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement Accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment Data Pointer	1	2
MUL	AB	Multiply A & B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal Adjust Accumulator	1	1

LOGICAL OPERATIONS

Mnemonic		Destination	Byte	Cyc
ANL	A,Rn	AND register to Accumulator	1	1
ANL	A,direct	AND direct byte to Accumulator	2	1
ANL	A,@Ri	AND indirect RAM to Accumulator	1	1
ANL	A,#data	AND immediate data to Accumulator	2	1
ANL	direct,A	AND Accumulator to direct byte	2	1
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to Accumulator	1	1
ORL	A,direct	OR direct byte to Accumulator	2	1
ORL	A,@Ri	OR indirect RAM to Accumulator	1	1
ORL	A,#data	OR immediate data to Accumulator	2	1
ORL	direct,A	OR Accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive-OR register to Accumulator	1	1
XRL	A,direct	Exclusive-OR direct byte to Accumulator	2	1
XRL	A,@Ri	Exclusive-OR indirect RAM to A	1	1
XRL	A,#data	Exclusive-OR immediate data to A	2	1
XRL	direct,A	Exclusive-OR Accumulator to direct byte	2	1
XRL	direct,#data	Exclusive-OR immediate data to direct	3	2
CLR	A	Clear Accumulator	1	1
CPL	A	Complement Accumulator	1	1
RL	A	Rotate Accumulator Left	1	1
RLC	A	Rotate A Left through the Carry flag	1	1
RR	A	Rotate Accumulator Right	1	1
RRC	A	Rotate A Right through Carry flag	1	1
SWAP	A	Swap nibbles within the Accumulator	1	1

DATA TRANSFER

Mnemonic		Description	Byte	Cyc
MOV	A,Rn	Move register to Accumulator	1	1
MOV	A,direct	Move direct byte to Accumulator	2	1
MOV	A,@Ri	Move indirect RAM to Accumulator	1	1
MOV	A,#data	Move immediate data to Accumulator	2	1
MOV	Rn,A	Move Accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move Accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct	3	2
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move Accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data16	Load Data Pointer with a 16-bit constant	3	2

DATA TRANSFER (cont.)

Mnemonic		Description	Byte	Cyc
MOVC	A,@A+DPTR	Move Code byte relative to DPTR to A	1	2
MOVC	A,@A+PC	Move Code byte relative to PC to A	1	2
MOVX	A,@Ri	Move External RAM (8-bit addr) to A	1	2
MOVX	A,@DPTR	Move External RAM (16-bit addr) to A	1	2
MOVX	@Ri,A	Move A to External RAM (8-bit addr)	1	2
MOVX	@DPTR,A	Move A to External RAM (16-bit addr)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with Accumulator	1	1
XCH	A,direct	Exchange direct byte with Accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with A	1	1
XCHD	A,@Ri	Exchange low-order Digit ind. RAM w A	1	1

BOOLEAN VARIABLE MANIPULATION

Mnemonic		Description	Byte	Cyc
CLR	C	Clear Carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set Carry flag	1	1
SETB	bit	Set direct Bit	2	1
CPL	C	Complement Carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to Carry flag	2	2
ANL	C, bit	AND complement of direct bit to Carry	2	2
ORL	C,bit	OR direct bit to Carry flag	2	2
ORL	C, bit	OR complement of direct bit to Carry	2	2
MOV	C,bit	Move direct bit to Carry flag	2	1
MOV	bit,C	Move Carry flag to direct bit	2	2

PROGRAM AND MACHINE CONTROL

Mnemonic		Description	Byte	Cyc
ACALL	addr11	Absolute Subroutine Call	2	2
LCALL	addr16	Long Subroutine Call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr11	Absolute Jump	2	2
LJMP	addr16	Long Jump	3	2
SJMP	rel	Short Jump (relative addr)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if Accumulator is Zero	2	2
JNZ	rel	Jump if Accumulator is Not Zero	2	2
JC	rel	Jump if Carry flag is set	2	2
JNC	rel	Jump if No Carry flag	2	2
JB	bit,rel	Jump if direct Bit set	3	2
JNB	bit,rel	Jump if direct Bit Not set	3	2
JBC	bit,rel	Jump if direct Bit is set & Clear bit	3	2
CJNE	A,direct,rel	Compare direct to A & Jump if Not Equal	3	2
CJNE	A,#data,rel	Comp. immed. to A & Jump if Not Equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. & Jump if Not Equal	3	2
CJNE	@Ri,#data,rel	Comp. immed. to ind. & Jump if Not Equal	3	2
DJNZ	Rn,rel	Decrement register & Jump if Not Zero	2	2
DJNZ	direct,rel	Decrement direct & Jump if Not Zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn	Working register R0-R7
direct	128 internal RAM locations, any I/O port, control or status register
@Ri	Indirect internal RAM location addressed by register R0 or R1
#data	8-bit constant included in instruction
#data16	16-bit constant included as bytes 2 & 3 of instruction
bit	128 software flags, any I/O pin, control or status bit

Notes on program addressing modes:

addr16	Destination address for LCALL & LJMP may be anywhere within the 64-Kilobyte program memory address space.
addr11	Destination address for ACALL & AJMP will be within the same 2-Kilobyte page of program memory as the first byte of the following instruction.
rel	SJMP and all conditional jumps include an 8-bit offset byte. Range is +127 -128 bytes relative to first byte of the following instruction.

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Table 2. Instruction Opcodes in Hexadecimal Order

Hex Code	Number of Bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr,code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit addr,code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A,*#data*
25	2	ADD	A,*data addr*
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	*bit addr,code addr*
31	2	ACALL	*code addr*
32	1	RETI	
33	1	RLC	A
34	2	ADDC	A,*#data*
35	2	ADDC	A,*data addr*
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R7
3F	1	ADDC	A,R7
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr*,A
43	3	ORL	*data addr,#data*
44	2	ORL	A,*#data*
45	2	ORL	A,*data addr*
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr*,A
53	3	ANL	*data addr,#data*
54	2	ANL	A,*#data*
55	2	ANL	A,*data addr*
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr*,A
63	3	XRL	*data addr,#data*
64	2	XRL	A,*#data*
65	2	XRL	A,*data addr*
66	1	XRL	A,@R0
67	1	XRL	A,@R1
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C,*bit addr*
73	1	JMP	@A+DPTR
74	2	MOV	A,*#data*
75	3	MOV	*data addr,#data*
76	2	MOV	@R0,*#data*
77	2	MOV	@R1,*#data*
78	2	MOV	R0,*#data*
79	2	MOV	R1,*#data*
7A	2	MOV	R2,*#data*
7B	2	MOV	R3,*#data*
7C	2	MOV	R4,*#data*
7D	2	MOV	R5,*#data*
7E	2	MOV	R6,*#data*
7F	2	MOV	R7,*#data*
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C,*bit addr*
83	1	MOVC	A,@A+PC

Table 2. Instruction Opcodes in Hexadecimal Order (Continued)

Hex Code	Number of Bytes	Mnemonic	Operands
84	1	DIV	AB
85	3	MOV	*data addr,data addr*
86	2	MOV	*data addr*,@R0
87	2	MOV	*data addr*,@R1
88	2	MOV	*data addr*,R0
89	2	MOV	*data addr*,R1
8A	2	MOV	*data addr*,R2
8B	2	MOV	*data addr*,R3
8C	2	MOV	*data addr*,R4
8D	2	MOV	*data addr*,R5
8E	2	MOV	*data addr*,R6
8F	2	MOV	*data addr*,R7
90	3	MOV	DPTR,#*data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr*,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#*data*
95	2	SUBB	A,*data addr*
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/*bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C,*bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,*data addr*
A7	2	MOV	@R1,*data addr*
A8	2	MOV	R0,*data addr*
A9	2	MOV	R1,*data addr*
AA	2	MOV	R2,*data addr*
AB	2	MOV	R3,*data addr*
AC	2	MOV	R4,*data addr*
AD	2	MOV	R5,*data addr*
AE	2	MOV	R6,*data addr*
AF	2	MOV	R7,*data addr*
B0	2	ANL	C,/*bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A,#*data,code addr*
B5	3	CJNE	A,*data addr,code addr*
B6	3	CJNE	@R0,#*data,code addr*
B7	3	CJNE	@R1,#*data,code addr*
B8	3	CJNE	R0,#*data,code addr*
B9	3	CJNE	R1,#*data,code addr*
BA	3	CJNE	R2,#*data,code addr*
BB	3	CJNE	R3,#*data,code addr*
BC	3	CJNE	R4,#*data,code addr*
BD	3	CJNE	R5,#*data,code addr*
BE	3	CJNE	R6,#*data,code addr*
BF	3	CJNE	R7,#*data,code addr*
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A

Hex Code	Number of Bytes	Mnemonic	Operands
C5	2	XCH	A,*data addr*
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr,code addr*
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,*code addr*
D9	2	DJNZ	R1,*code addr*
DA	2	DJNZ	R2,*code addr*
DB	2	DJNZ	R3,*code addr*
DC	2	DJNZ	R4,*code addr*
DD	2	DJNZ	R5,*code addr*
DE	2	DJNZ	R6,*code addr*
DF	2	DJNZ	R7,*code addr*
E0	1	MOVX	A,@DPTR
E1	2	AJMP	*code addr*
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,*data addr*
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	*code addr*
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	*data addr*,A
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

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Ordering Information

Part Number	Temperature Range	Package Type	Rom
P - 8051	0° – 70° C	PLASTIC	4K × 8
D - 8051	0° – 70° C	CERDIP	4K × 8
P - 8031	0° – 70° C	PLASTIC	EXTERNAL
D - 8031	0° – 70° C	CERDIP	EXTERNAL

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MATRA-HARRIS SEMICONDUCTEURS

data sheet

intel

I 8031 / I 8051
SINGLE-COMPONENT 8-BIT MICROCOMPUTER

PRELIMINARY

INDUSTRIAL

SEPTEMBER 1983

- I 8031 - Control Oriented CPU With RAM and I/O
- I 8051 - An I 8031 With Factory Mask-Programmable ROM
- Industrial Temperature Range : − 40° C to + 85° C

- 4K × 8 ROM
- 128 × 8 RAM
- Four 8-Bit Ports, 32 I/O Lines
- Two 16-Bit Timer/Event Counters
- High-Performance Full-Duplex Serial Channel
- External Memory Expandable to 128K
- Compatible with MCS-80® /MCS-85® Peripherals
- Boolean Processor
- MCS-48® Architecture Enhanced with :
  - Non-Paged Jumps
  - Direct Addressing
  - Four 8-Register Banks
  - Stack Depth Up to 128-Bytes
  - Multiply, Divide, Subtract, Compare
- Most Instructions Execute in 1 μs
- 4 μs Multiply and Divide

The MHS I 8031/I 8051 is a stand-alone, high-performance single-chip computer fabricated with MHS highly-reliable + 5 Volt, depletion-load, N-Channel, silicon-gate HMOS technology and packaged in a 40-pin DIP. It provides the hardware features, architectural enhancements and new instructions that are necessary to make it a powerful and cost effective controller for applications requiring up to 64K bytes of program memory and/or up to 64K bytes of data storage.

The I 8051 contains a non-volatile 4K × 8 read-only program memory; a volatile 128 × 8 read/write data memory 32 I/O lines; two 16-bit timer/counters; a five-source, two-priority-level, nested interrupt structure; a serial I/O port for either multi-processor communications, I/O expansion, or full duplex UART; and on-chip oscillator and clock circuits. The I 8031 is identical, except that it lacks the program memory. For systems that require extra capability, the I 8051 can be expanded using standard TTL compatible memories and the byte oriented MCS-80® and MCS-85® peripherals.

The I 8051 microcomputer, like its I 8048 predecessor, is efficient both as a controller and as an arithmetic processor. The I 8051 has extensive facilities for binary and BCD arithmetic and excels in bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 12 MHz crystal, 58% of the instructions execute in 1.0 μs, 40% in 2.0 μs and multiply and divide require only 4.0 μs. Among the many instructions added to the standard I 8048 instruction set are multiply, divide, subtract and compare.

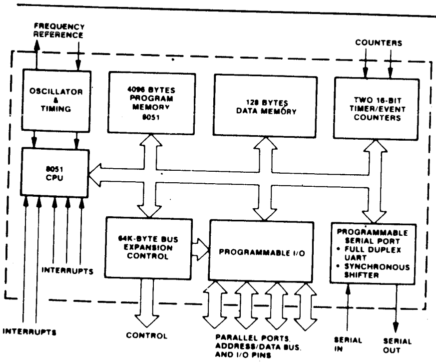

Figure 1.
Block Diagram

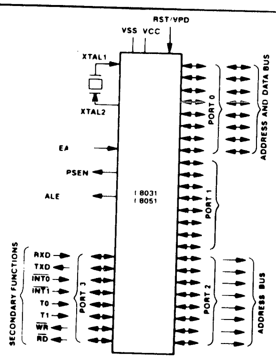

Figure 2.
Logic Symbol

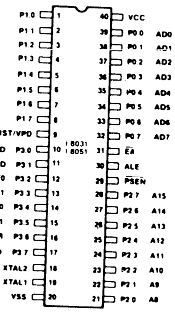

Figure 3. Pin Configuration

For a complete description of I 8031/I 8051 features and operating characteristics, refer to the standard commercial grade data sheet. This document highlights only the electrical specifications which differ from the commercial part.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . − 40° C to 85° C
Storage Temperature . . . . − 65° C to + 150° C
Voltage on Any Pin With
Respect to Ground (Vss) . . . . . . − 0,5 V to + 7 V
Power Dissipation . . . . 2 Watts

**NOTICE : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Extended Temperature Electrical Deviations to Commercial Specifications

D.C. CHARACTERISTICS (TA = − 40° C to 85° C; VCC = 4.75 V to 5.25 V; VSS = 0 V)

Symbol	Parameter	Limits Min	Limits Max	Unit	Test Conditions
VIL	Input Low Voltage (all except XTAL2)	− 0.5	0.7	V	
VIH	Input High Voltage (except XTAL2, RST/VPD)	2.1	VCC + 0.5	V	
VOL	Output Low Voltage Ports 1, 2, 3 (Note 1)		0.45	V	IOL = 1.2 mA
VOL1	Output Low Voltage Port 0, ALE, PSEN (Note 1)		0.45	V	IOL = 2.4 mA
VOH	Output High Voltage Ports 1, 2, 3	2.4		V	IOH = − 60 μA
VOH1	Output High Voltage ALE, PSEN, Port 0	2.4		V	IOH = − 320 μA
IIL	Logical 0 Input Current P1, P2, P3, ALE, PSEN		− 1.2	mA	VIL = 0.45 V
IIL2	Logical 0 Input Current XTAL2		− 2.8	mA	XTAL1 at VSS VIL = 0.45 V
ICC	Power Supply Current		175	mA	All Outputs Disconnected EA = VCC

Note 1 : VOL is degraded when the I 8051 rapidly discharges external capacitance. This A.C. noise is most pronounced during emission of address data. When using external memory, locate the latch or buffer as close to the I 8051 as possible.

Datum	Emitting Ports	Degraded I/O Lines	VOL (Peak) (max)
Address	P2, P0	P1, P3	0.8 V
Write Data	P0	P1, P3, ALE	0.8 V

Ordering Information

Part Number	Temperature Range	Package Type	Rom
IP - 8051	- 40°C to 85°C	PLASTIC	4K × 8
ID - 8051	- 40°C to 85°C	CERDIP	4K × 8
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MATRA-HARRIS SEMICONDUCTEURS

data sheet

intel

M 8031/M 8051
SINGLE-COMPONENT 8-BIT MICROCOMPUTE

PRELIMINARY

MILITARY

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- Military Temperature Range : − 55° C to + 125° C

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- Two 16-Bit Timer/Event Counters
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- External Memory Expandable to 128K
- Compatible with MCS-80® /MCS-85® Peripherals
- Boolean Processor
- MCS-48® Architecture Enhanced with :
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  - Direct Addressing
  - Four 8-Register Banks
  - Stack Depth Up to 128-Bytes
  - Multiply, Divide, Subtract, Compare
- Most Instructions Execute in 1 μs
- 4 μs Multiply and Divide

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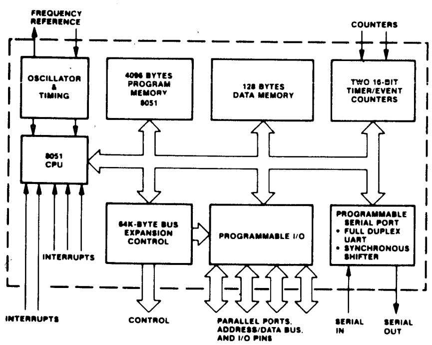

Figure 1.
Block Diagram

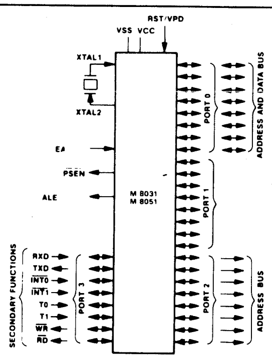

Figure 2.
Logic Symbol

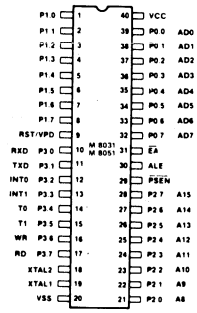

Figure 3. Pin Configuration

For a complete description of M 8031/M 8051 features and characteristics, refer to the standard commercial grade data sheet.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . − 55° C to 125° C
Storage Temperature . . . . − 65° C to + 150° C
Voltage on Any Pin With
Respect to Ground (Vss) . . . . . . − 0,5 V to + 7 V
Power Dissipation . . . . 2 Watts

**NOTICE : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC CHARACTERISTICS (TA = − 55° C to 125° C; VCC = 4.75 V to 5.25 V; VSS = 0 V)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
VIL	Input Low Voltage	−0.5		0.7	V	
VIH	Input High Voltage (Except RST/VPD and XTAL2)	2.1		VCC+0.5	V	
VIH1	Input High Voltage To RST/VPD For Reset, XTAL2	2.8			V	XTAL1 to VSS
VPD	Power Down Voltage To RST/VPD	4.5		5.5	V	VCC = 0 V
VOL	Output Low Voltage Ports 1, 2, 3 (Note 1)			0.45	V	IOL = 1.6 mA
VOL1	Output Low Voltage Port 0, ALE, /PSEN (Note 1)			0.45	V	IOL = 3.2 mA
VOH	Output High Voltage Ports 1, 2, 3	2.4			V	IOH = − 60 μA
VOH1	Output High Voltage Port 0, ALE, /PSEN	2.4			V	IOH = − 400 μA
IIL	Logical 0 Input Current XTAL 2, Ports 1, 2, 3			− 900	μA	XTAL1 at VSS VIL = 0.45 V
IIH1	Input High Current To RST/VPD For Reset			600	μA	Vin = VCC − 1.5 V
ILI	Input Leakage Current To Port 0, /EA			10	μA	0<Vin<VCC
ICC	Power Supply Current		125	190	mA	
IPD	Power Down Current		10	20	mA	
CIO	Capacitance of I/O Buffer			10	pF	fc = 1 MHz

Note 1 : VOL is degraded when the M 8051 rapidly discharges external capacitance. This A.C. noise is most pronounced during emission of address data. When using external memory, locate the latch or buffer as close to the M 8051 as possible.

Datum	Emitting Ports	Time Interval	Degraded I/O Lines	VOL (peak) (max)
Address	P2, P0	T3, T9	P1, P3	.8 V
Write Data	P0	T6	P1, P3, ALE	.8 V

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A.C. CHARACTERISTICS (TA − 55° C to 125° C; VCC = 5 V ± 5%; Vss = 0 V; CL for Port 0, ALE and PSEN Outputs = 100 pF; CL for All Other Outputs = 80 pF).

Program Memory Characteristics

Symbol	Parameter	12 MHz Clock			Variable Clock 1/TCLCL = 1.2 MHz to 12 MHz		
		Min	Max	Units	Min	Max	Units
TLHLL	ALE Pulse Width	127		ns	2TCLCL− 40		ns
TAVLL	Address Setup to ALE	43		ns	TCLCL− 40		ns
TLLAX	Address Hold After ALE	38		ns	TCLCL− 45		ns
TLLIV	ALE To Valid Instr In		198	ns		4TCLCL−135	ns
TLLPL	ALE to PSEN	58		ns	TCLCL− 25		ns
TPLPH	PSEN Pulse Width	215		ns	3TCLCL− 35		ns
TPLIV	PSEN To Valid Instr In		115	ns		3TCLCL−135	ns
TPXIX	Input Instr Hold After PSEN	0		ns	0		ns
*TPXIZ	Input Instr Float After PSEN		63	ns		TCLCL− 20	ns
*TPXAV	Address Valid After PSEN	70		ns	TCLCL− 13		ns
TAVIV	Address To Valid Instr In		267	ns		5TCLCL−150	ns
TAZPL	Address Float To PSEN	0		ns	0		ns

***NOTE 1 :** Interfacing the M 8051 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers.

External Data Memory Characteristics

Symbol	Parameter	12 MHz Clock			Variable Clock 1/TCLCL = 1.2 MHz to 12 MHz		
		Min	Max	Units	Min	Max	Units
TRLRH	RD Pulse Width	400		ns	6TCLCL−100		ns
TWLWH	WR Pulse Width	400		ns	6TCLCL−100		ns
TLLAX	Address Hold After ALE	48		ns	TCLCL− 35		
TRLDV	RD To Valid Data In		250	ns		5TCLCL−165	ns
TRHDX	Data Hold After RD	0		ns	0		ns
TRHDZ	Data Float After RD		97	ns		2TCLCL− 70	ns
TLLDV	ALE To Valid Data In		517	ns		8TCLCL−150	ns
TAVDV	Address To Valid Data In		585	ns		9TCLCL−165	ns
TLLWL	ALE To WR or RD	200	300	ns	3TCLCL− 50	3TCLCL+ 50	ns
TAVWL	Address To WR or RD	203		ns	4TCLCL−130		ns
TWHLH	WR or RD High To ALE High	43	123	ns	TCLCL− 40	TCLCL+ 40	ns
TDVWX	Data Valid To WR Transition	33		ns	TCLCL− 50		ns
TQVWH	Data Setup Before WR	433		ns	7TCLCL−150		ns
TWHQX	Data Hold After WR	33		ns	TCLCL− 50		ns
TRLAZ	Address Float After RD		0	ns		0	ns

Ordering Information

Part Number	Temperature Range	Package Type	Rom	Burn-in Hours
MD - 8051	− 55°C to 125°C	CERDIP	4K × 8	0
MD - 8051/B	− 55°C to 125°C	CERDIP	4K × 8	168
MD - 8031	− 55°C to 125°C	CERDIP	EXTERNAL	0
MD - 8031/B	− 55°C to 125°C	CERDIP	EXTERNAL	168

MHS
MATRA-HARRIS SEMICONDUCTEURS
data sheet

8048 H/8035 H
HMOS SINGLE COMPONENT 8-BIT MICROCOMPUTER

PRELIMINARY

8048H/8048H Mask Programmable ROM
8035H/8035H CPU Only with Power Down Mode
8035HL-1

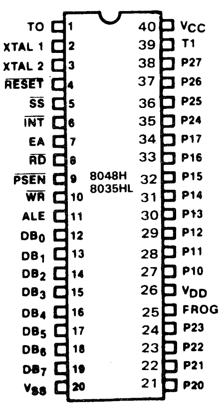
- **8-BIT CPU, ROM, RAM, I/O in Single Package**
- **High Performance HMOS**
- **Reduced Power Consumption**
- **1.4μ sec and 1.9μ sec Cycle Versions All Instructions 1 or 2 Cycles.**
- **Over 96 Instructions: 90% Single Byte**
- **1K x 8 ROM**
  64 x 8 RAM
  27 I/O Lines
- **Interval Timer/Event Counter**
- **Easily Expandable Memory and I/O**
- **Compatible with 8080/8085 Series Peripherals**
- **Two Single Level Interrupts**

The MHS 8048H/8048H-1/8035HL/8035HL-1 are totally self-sufficient, 8-bit parallel computers fabricated on single silicon chips using Intel's advanced N-channel silicon gate HMOS process.

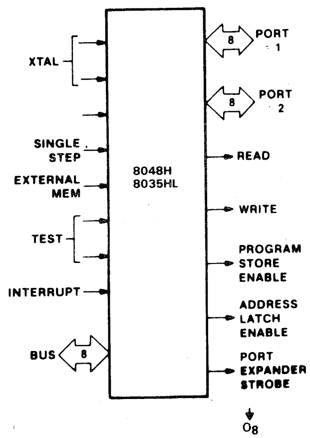
The 8048H contains a 1K X 8 program memory, a 64 X 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on-board oscillator and clock circuits. For systems that require extra capability the 8048H can be expanded using standard memories and MCS-80™/MCS-85™ peripherals. The 8035HL is the equivalent of the 8048H without program memory and can be used with external ROM AND RAM.

These microcomputers are designed to be efficient controllers as well as arithmetic processors. They have extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single bit instructions and no instructions over 2 bytes in length.

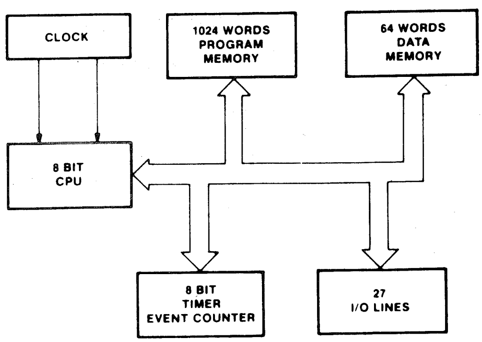
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



Instruction Set (Cont.)

Mnemonic	Function	Description	Instruction Code D7	D6	D5	D4	D3	D2	D1	D0	Cycles	Bytes	Flags C	AC	F0	F1
Branch (Cont.)																
JNT0 addr	(PC 0 - 7) ← addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if Test 0 is low.	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNT1 addr	(PC 0 - 7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if Test 1 is low.	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNZ addr	(PC 0 - 7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 0	Jump to specified addres if Accumulator is non-zero.	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JTF addr	(PC 0 - 7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if Timer Flag is set to 1.	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT0 addr	(PC 0 - 7) ← addr if T0 = 1 (PC) ← (PC) + 2 if T0 = 0	Jump to specified address if Test 0 is a 1.	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT1 addr	(PC 0 - 7) ← addr if T1 = 1 (PC) ← (PC) - 2 if T1 = 0	Jump to specified address if Test 1 is a 1.	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JZ addr	(PC 0 - 7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if Accumulator is 0.	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
Control																
EN I		Enable the External Interrupt input.	0	0	0	0	0	1	0	1	1	1				
DIS I		Disable the External Interrupt input.	0	0	0	1	0	1	0	1	1	1				
ENT0 CLK		Enable the Clock Output pin T0.	0	1	1	1	0	1	0	1	1	1				
SEL MB0	(DBF) ← 0	Select Bank 0 (locations 0 - 2047) of Program Memory.	1	1	1	0	0	1	0	1	1	1				
SEL MB1	(DBF) ← 1	Select Bank 1 (locations 2048 - 4095) of Program Memory.	1	1	1	1	0	1	0	1	1	1				
SEL RB0	(BS) ← 0	Select Bank 0 (locations 0 - 7) of Data Memory.	1	1	0	0	0	1	0	1	1	1				
SEL RB1	(BS) ← 1	Select Bank 1 (locations 24 - 31) of Data Memory.	1	1	0	1	0	1	0	1	1	1				
Data Moves																
MOV A, # data	(A) ← data	Move Immediate the specified data into the Accumulator.	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
MOV A, Rr	(A) ← (Rr); r = 0 - 7	Move the contents of the designated registers into the Accumulator.	1	1	1	1	1	r	r	r	1	1				
MOV A, @ Rr	(A) ← ((Rr)); r = 0 - 1	Move Indirect the contents of data memory location into the Accumulator.	1	1	1	1	0	0	0	r	1	1				
MOV A, PSW	(A) ← (PSW)	Move contents of the Program Status Word into the Accumulator.	1	1	0	0	0	1	1	1	1	1				
MOV Rr, = data	(Rr) ← data; r = 0 - 7	Move Immediate the specified data into the designated register.	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2				
MOV Rr, A	(Rr) ← (A); r = 0 - 7	Move Accumulator Contents into the designated register.	1	0	1	0	1	r	r	r	1	1				
MOV @ Rr, A	((Rr)) ← (A), r = 0 - 1	Move Indirect Accumulator Contents into data memory location.	1	0	1	0	0	0	0	r	1	1				
MOV @ Rr, = data	((Rr)) ← data; r = 0 - 1	Move Immediate the specified data into data memory.	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2				
MOV PSW, A	(PSW) ← (A)	Move contents of Accumulator into the program status word.	1	1	0	1	0	1	1	1	1	1				
MOVP A, @ A	(PC 0 - 7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator.	1	0	1	0	0	0	1	1	2	1				
MOVP3 A, @ A	(PC 0 - 7) ← (A) (PC 8 - 10) ← 011 (A) ← ((PC))	Move Program data in Page 3 into the Accumulator.	1	1	1	0	0	0	1	1	2	1				
MOVX A, @ R	(A) ← ((Rr)); r = 0 - 1	Move Indirect the contents of external data memory into the Accumulator.	1	0	0	0	0	0	0	r	2	1				
MOVX @ R, A	((Rr)) ← (A), r = 0 - 1	Move Indirect the contents of the Accumulator into external data memory.	1	0	0	1	0	0	0	r	2	1				
XCH A, Rr	(A) ⇄ (Rr); r = 0 - 7	Exchange the Accumulator and designated register's contents.	0	0	1	0	1	r	r	r	1	1				
XCH A, @ Rr	(A) ← ((Rr)); r = 0 - 1	Exchange Indirect contents of Accumulator and location in data memory.	0	0	1	0	0	0	0	r	1	1				
XCHD A, @ Rr	(A 0 - 3) ⇄ ((Rr)) 0 - 3)); r = 0 - 1	Exchange Indirect 4 bit contents of Accumulator and data memory.	0	0	1	1	0	0	0	r	1	1				
Flags																
CPL C	(C) ← NOT (C)	Complement carry bit.	1	0	1	0	0	1	1	1	1	1	•			
CPL F0	(F0) ← NOT (F0)	Complement Flag F0.	1	0	0	1	0	1	0	1	1	1			•	
CPL F1	(F1) ← NOT (F1)	Complement of Flag F 1.	1	0	1	1	0	1	0	1	1	1				•
CLR C	(C) ← 0	Clear carry bit to 0.	1	0	0	1	0	1	1	1	1	1	•			
CLR F0	(F0) ← 0	Clear Flag 0 to 0.	1	0	0	0	0	1	0	1	1	1			•	
CLR F1	(F1) ← 0	Clear Flag 1 to 0.	1	0	1	0	0	1	0	1	1	1				•

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Instruction Set

Mnemonic	Function	Description	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1
Accumulator																
ADD, A = data	(A) ← (A) + data	Add immediate the specified Data to the Accumulator.	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•			
Add A, Rr	(A) ← (A) + (Rr) for r = 0 - 7	Add contents of designated register to the Accumulator.	0	1	1	0	1	r	r	r	1	1	•			
ADD A, @ Rr	(A) ← (A) + ((Rr)) for r = 0 - 1	Add indirect the contents of the data memory location to the Accumulator.	0	1	1	0	0	0	0	r	1	1	•			
ADDC A, = data	(A) ← (A) + (C) + data	Add immediate with carry the specified data to the Accumulator.	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•			
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0 - 7	Add with carry the contents of the designated register to the Accumulator.	0	1	1	1	1	r	r	r	1	1	•			
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0 - 1	Add indirect with carry the contents of data memory location to the Accumulator.	0	1	1	1	0	0	0	r	1	1	•			
ANL A, = data	(A) ← (A) AND data	Logical AND specified Immediate Data with Accumulator.	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0 - 7	Logical AND contents of designated register with Accumulator.	0	1	0	1	1	r	r	r	1	1				
ANL A, @ Rr	(A) ← (A) AND ((Rr)) for r = 0 - 1	Logical AND Indirect the contents of data memory with Accumulator.	0	1	0	1	0	0	0	r	1	1				
CPL A	(A) ← NOT (A)	Complement the contents of the Accumulator.	0	0	1	1	0	1	1	1	1	1				
CLR A	(A) ← 0	Clear the contents of the Accumulator.	0	0	1	0	0	1	1	1	1	1				
DA A		Decimal Adjust the contents of the Accumulator.	0	1	0	1	0	1	1	1	1	1	•			
DEC A	(A) ← (A) − 1	Decrement by 1 the Accumulator's contents.	0	0	0	0	0	1	1	1	1	1				
INC A	(A) ← (A) + 1	Increment by 1 the Accumulator's contents.	0	0	0	1	0	1	1	1	1	1				
ORL A, = data	(A) ← (A) OR data	Logical OR specified immediate data with Accumulator.	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0 - 7	Logical OR contents of designated register with Accumulator.	0	1	0	0	1	r	r	r	1	1				
ORL A, @ Rr	(A) ← (A) OR ((Rr)) for r = 0 - 1	Logical OR Indirect the contents of data memory location with Accumulator.	0	1	0	0	0	0	0	r	1	1				
RL A	(AN + 1) ← (AN) (A_0) ← (A_7) for N = 0 - 6	Rotate Accumulator left by 1 bit without carry.	1	1	1	0	0	1	1	1	1	1				
RLC A	(AN + 1) ← (AN); N = 0 - 6 (A_0) ← (C) (C) ← (A_7)	Rotate Accumulator left by 1 bit through carry.	1	1	1	1	0	1	1	1	1	1	•			
RR A	(AN) ← (AN + 1), N = 0 - 6 (A_7) ← (A_0)	Rotate Accumulator right by 1 bit without carry.	0	1	1	1	0	1	1	1	1	1				
RRC A	(AN) ← (AN + 1); N = 0 - 6 (A_7) ← (C) (C) ← (A_0)	Rotate Accumulator right by 1 bit through carry.	0	1	1	0	0	1	1	1	1	1	•			
SWAP A	(A_{4-7}) ⇄ (A_0-3)	Swap the two 4-bit nibbles in the Accumulator.	0	1	0	0	0	1	1	1	1	1				
XRL A, = data	(A) ← (A) XOR data	Logical XOR specified immediate data with Accumulator.	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0 - 7	Logical XOR contents of designated register with Accumulator.	1	1	0	1	1	r	r	r	1	1				
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0 - 1	Logical XOR Indirect the contents of data memory location with Accumulator.	1	1	0	1	0	0	0	r	1	1				
Branch																
DJNZ Rr, addr	(Rr) ← (Rr) - 1; r = 0 - 7 If (Rr) ≠ 0 (PC 0 - 7) ← addr	Decrement the specified register and test contents.	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2				
JBb addr	(PC 0 - 7) ← addr if Bb = 1 (PC) - (PC) + 2 if Bb = 0	Jump to specified address if Accumulator bit is set.	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2				
JC addr	(PC 0 - 7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF 0 addr	(PC 0 - 7) ← addr if FO = 1 (PC) ← (PC) + 2 if FO = 0	Jump to specified address if Flag F 0 is set.	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF 1 addr	(PC 0 - 7) ← addr if F 1 = 1 (PC) ← (PC) + 2 if F 1 = 0	Jump to specified address if Flag F 1 is set.	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JMP addr	(PC 8 - 10) ← addr 8 − 10 (PC 0 - 7) ← addr 0 - 7 (PC 11) ← DBF	Direct Jump to specified address within the 2K address block.	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2				
JMPP @ A	(PC 0 7) ← ((A))	Jump indirect to specified address with address page.	1	0	1	1	0	0	1	1	2	1				
JNC addr	(PC 0 7) ← addr if C 0 (PC) ← (PC) + 2 if C 1	Jump to specified address if carry flag is low.	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNI addr	(PC 0 7) ← addr if I 0 (PC) ← (PC) + 2 if 1	Jump to specified address if interrupt is low.	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				

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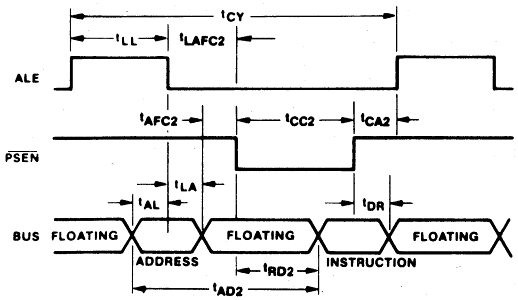
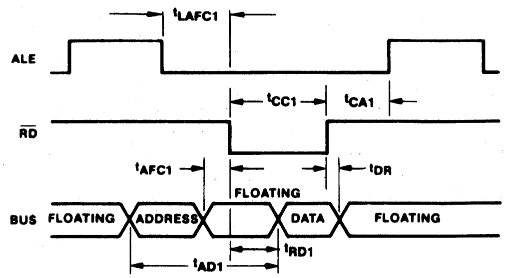
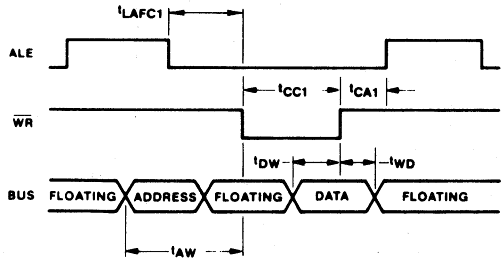
WAVEFORMS



Instruction Fetch From External Program Memory



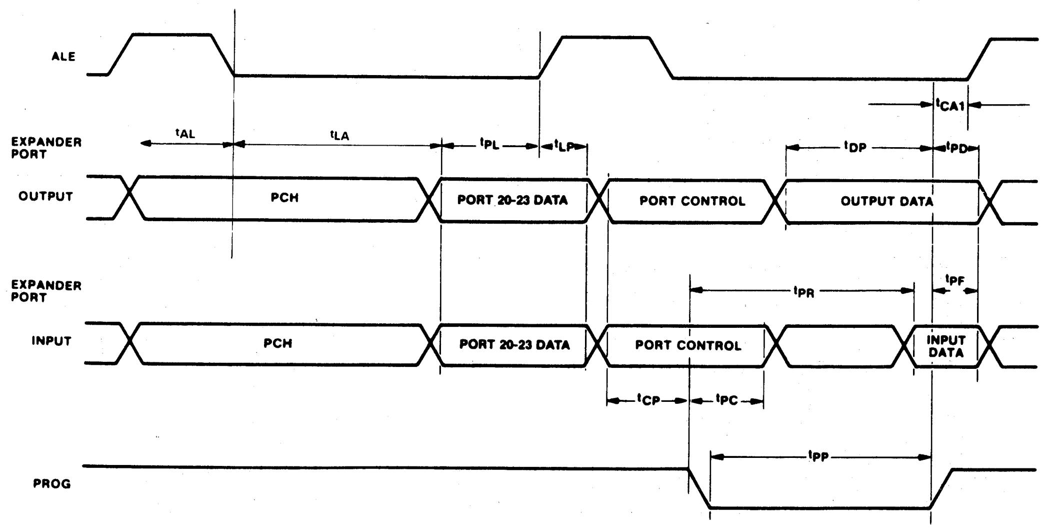
Read From External Data Memory



Write to External Data Memory

Input and Output for A.C.Tests

PORT 2 TIMING



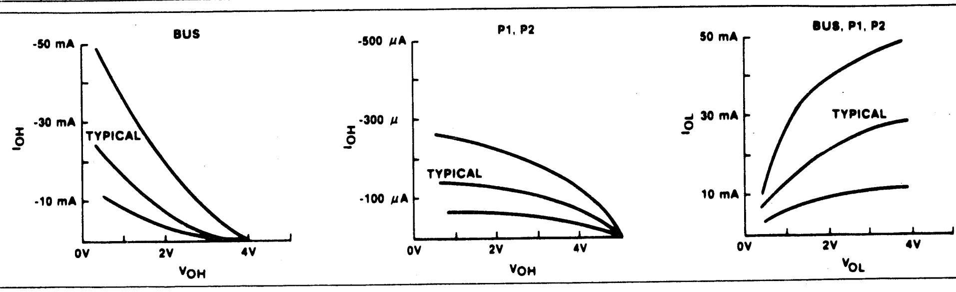
ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias .... 0°C to 70°C
Storage Temperature .... -65°C to +150°C
Voltage On Any Pin With Respect
  to Ground .... -0.5V to +7V
Power Dissipation .... 1.5 Watt

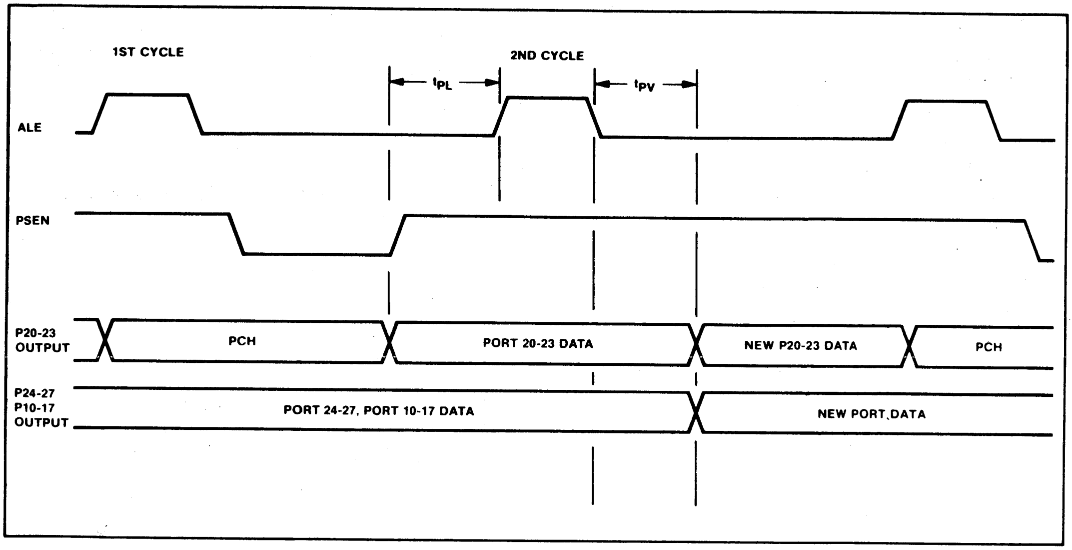
**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

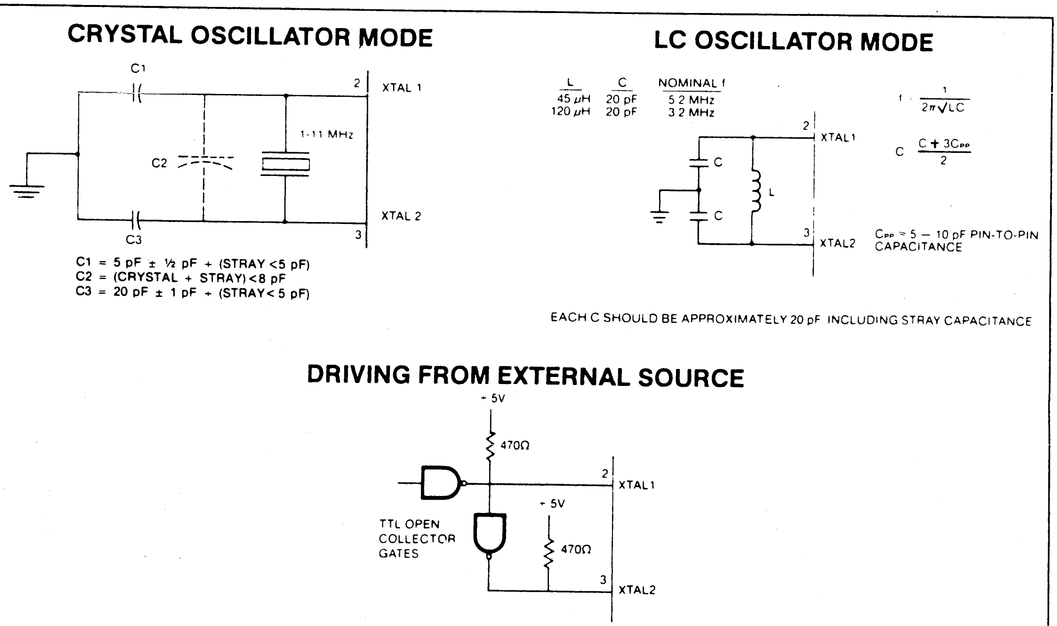
D.C. CHARACTERISTICS (TA = 0°C to 70°C, V_{CC} = V_{DD} = 5V + 10%, V_{SS} = 0V)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
V_{IL}	Input Low Voltage (All Except $\overline{RESET}$, X1, X2)	-.5		.8	V	
V_{IL1}	Input Low Voltage ($\overline{RESET}$, X1, X2)	-.5		.6	V	
V_{IH}	Input High Voltage (All Except XTAL1, XTAL2, $\overline{RESET}$)	2.0		V_{CC}	V	
V_{IH1}	Input High Voltage (X1, X2, $\overline{RESET}$)	3.8		V_{CC}	V	
V_{OL}	Output Low Voltage (BUS)			.45	V	I_{OL} = 2.0 mA
V_{OL1}	Output Low Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)			.45	V	I_{OL} = 1.8 mA
V_{OL2}	Output Low Voltage (PROG)			.45	V	I_{OL} = 1.0 mA
V_{OL3}	Output Low Voltage (All Other Outputs)			.45	V	I_{OL} = 1.6 mA
VOH	Output High Voltage (BUS)	2.4			V	I_{OH} = -400μA
V_{OH1}	Output High Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	2.4			V	I_{OH} = -100μA
V_{OH2}	Output High Voltage (All Other Outputs)	2.4			V	I_{OH} = -40μA
I_{L1}	Input Leakage Current (T1, $\overline{INT}$)			± 10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
I_{LI1}	Input Leakage Current (P10-P17, P20-P27, EA, $\overline{SS}$)			-500	μA	V_{SS} + .45 $\leq V_{IN} \leq V_{CC}$
I_{LO}	Output Leakage Current (BUS, TO) (High Impedance State)			± 10	μA	V_{SS} + .45 $\leq V_{IN} \leq V_{CC}$
I_{DD}	V_{DD} Supply Current		4	8	mA	
I_{DD} + I_{CC}	Total Supply Current		40	80	mA	
V_{DD}	RAM Standby Pin Voltage	2.2		5.5	V	Standby Mode, Reset ≤0.6V



I/O PORT TIMING





FOR XTAL 1 AND XTAL 2 DEFINE "HIGH" AS VOLTAGES ABOVE 1.6V AND "LOW" AS VOLTAGES BELOW 1.6V. THE DUTY CYCLE REQUIREMENTS FOR EXTERNALLY DRIVING XTAL 1 AND XTAL 2 USING THE CIRCUIT SHOWN ABOVE ARE AS FOLLOWS:

XTAL 1 MUST BE HIGH 35 TO 65% OF THE PERIOD AND XTAL 2 MUST BE HIGH 35 TO 65% OF THE PERIOD. RISE AND FALL TIMES MUST BE FASTER THAN 20 nS.

5

A.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = V_{DD} = 5V ± 10%, V_{SS} = OV)

Symbol	Parameter	F (t_{CY})	8048H 8035HL 6 MHz Min	8048H 8035HL 6 MHz Max	8048H 8035HL 8 MHz Min	8048H 8035HL 8 MHz Max	8048H-1 8035HL-1 11 MHz Min	8048H-1 8035HL-1 11 MHz Max	Unit	Conditions (Note 1)
t_{LL}	ALE Pulse Width	7/30 t_{CY} -170	400		260		150		ns	
t_{AL}	Addr Setup to ALE	2/15 t_{CY}-110	220		140		70			(Note 2)
t_{LA}	Addr Hold from ALE	1/15 t_{CY} -40	120		80		50			
t_{CC1}	Control Pulse Width ($\overline{RD}$, $\overline{WR}$)	1/2 t_{CY} -200	1050		730		480			
t_{CC2}	Control Pulse Width ($\overline{PSEN}$)	2/5 t_{CY} -200	800		550		350			
t_{DW}	Data Setup before $\overline{WR}$	13/30 t_{CY} -200	880		610		390			
t_{WD}	Data Hold after $\overline{WR}$	1/15 t_{CY} -50	166		75		40			(Note 2)
t_{DR}	Data Hold ($\overline{RD}$, $\overline{PSEN}$)	1/10 t_{CY} -30	0	220	0	160	0	110		
t_{RD1}	$\overline{RD}$ to Data in	11/30 t_{CY}-170		750		510		330		
t_{RD2}	$\overline{PSEN}$ to Data in	4/15 t_{CY}-170		500		330		190		
t_{AW}	Addr Setup to $\overline{WR}$	1/3 t_{CY}-150	700		475		300			
t_{AD1}	Addr Setup to Data ($\overline{RD}$)	7/10 t_{CY}-220		1530		1100		730		
t_{AD2}	Addr Setup to Data ($\overline{PSEN}$)	1/2 t_{CY}-220		1250		880		460		
t_{AFC1}	Addr Float to $\overline{RD}$, $\overline{WR}$	2/15 t_{CY} -40	290		210		140			(Note 2)
t_{AFC2}	Addr Float to $\overline{PSEN}$	1/30 t_{CY} -40	40		20		10			(Note 2)
t_{LAFC1}	ALE to Control ($\overline{RD}$, $\overline{WR}$)	1/5 t_{CY} -75	420		300		200			
t_{LAFC2}	ALE to Control ($\overline{PSEN}$)	1/10 t_{CY} -75	170		110		60			
t_{CA1}	Control to ALE ($\overline{RD}$, $\overline{WR}$, $\overline{PROG}$)	1/15 t_{CY} -40	120		80		50			
t_{CA2}	Control to ALE ($\overline{PSEN}$)	4/15 t_{CY} -40	620		460		320			
t_{CP}	Port Control Setup to $\overline{PROG}$	2/15 t_{CY} -80	210		140		100			
t_{PC}	Port Control Hold to $\overline{PROG}$	4/15 t_{CY} -200	460		300		160			
t_{PR}	$\overline{PROG}$ to P2 Input Valid	17/30 t_{CY}-120		1300		940		650		
t_{PF}	Input Data Hold from $\overline{PROG}$	1/10 t_{CY}		250	0	190	0	140		
t_{DP}	Output Data Setup	2/5 t_{CY} -150	850		600		400			
t_{PD}	Output Data Hold	1/10 t_{CY} -50	200		130		90			
t_{PP}	$\overline{PROG}$ Pulse Width	7/10 t_{CY} -250	1500		1060		700			
t_{PL}	Port 2 I/O Setup to ALE	4/15 t_{CY} -200	460		300		160			
t_{LP}	Port 2 I/O Hold to ALE	1/30 t_{CY}30	50		30		15			
t_{PV}	Port Output from ALE	3/10 t_{CY} +100		850		660		510		
t_{CY}	Cycle Time	15/F (XTAL)	2.5		1.875		1.36		μs	(Note 3)
t_{0PRR}	T0 Rep Rate	3/15 t_{CY}	500		370		270		ns	

Notes:
1. Control Outputs CL = 80pF
   BUS Outputs CL = 150pF
2. BUS High Impedance Load 20pF
3. f(t_{CY}) assumes 50% duty cycle on X1 and X2
   t_{CY} max = 15.0 μs

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Instruction Set (Cont.)

Mnemonic	Function	Description	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1
Input/Output																
ANL BUS, data	(BUS) ← (BUS) AND data	Logical AND immediate specified data with contents of Bus.	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2				
ANL P_p, data	(P_i) ← (P_i) AND data p 1 - 2	Logical AND immediate specified data with designated port (1 or 2).	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2				
ANLD P_p, A	(P_i) ← (P_i) AND (A0 - 3) p 4 - 7	Logical AND contents of Accumulator with designated port (4 - 7).	1	0	0	1	1	1	p	p	2	1				
IN A, P_p	(A) ← (P_i), p 1 - 2	Input data from designated port (1 - 2) into Accumulator.	0	0	0	0	1	0	p	p	2	1				
INS A, BUS	(A) ← (BUS)	Input strobed Bus data into Accumulator.	0	0	0	0	1	0	0	0	2	1				
MOVD A, P_p	(A 0 - 3) ← (P_i); p 4 - 7 (A 4 - 7) ← 0	Move contents of designated port (4 - 7) into Accumulator.	0	0	0	0	1	1	p	p	2	1				
MOVD P_p, A	(P_i) ← A 0 - 3; p 4 - 7	Move contents of Accumulator designated port (4 - 7).	0	1	1	1	1	p	p	1	1					
ORL BUS, data	(BUS) ← (BUS) OR data	Logical OR immediate specified data with contents of Bus.	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2				
ORLD P_p, A	(P_i) ← (P_i) OR (A0 - 3) P 4 - 7	Logical OR contents of Accumulator with designated port (4 - 7).	1	0	0	0	1	1	p	p	1	1				
ORL P_p, data	(P_i) ← (P_i) OR data p 1 - 2	Logical OR immediate specified data with designated port (1 - 2).	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2				
OUTL BUS, A	(BUS) ← (A)	Output contents of Accumulator onto Bus.	0	0	0	0	0	0	1	0	1	1				
OUTL P_p, A	(P_i) ← (A); p 1 - 2	Output contents of Accumulator to designated port (1 - 2).	0	0	1	1	1	0	p	p	1	1				
Registers																
DEC Rr (Rr)	(Rr) ← (Rr) 1; r 0 - 7	Decrement by 1 contents of designated register.	1	1	0	0	1	r	r	r	1	1				
INC Rr	(Rr) ← (Rr) + 1, r 0 - 7	Increment by 1 contents of designated register.	0	0	0	1	1	r	r	r	1	1				
INC @ R	((Rr)) ← ((Rr)) + 1; r 0 - 1	Increment Indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r	1	1				
Subroutine																
Call addr	((SP)) ← (PC), (PSW 4 - 7) (SP) ← (SP) + 1 (PC 8 - 10) ← addr 8 - 10 (PC 0 - 7) ← addr 0 - 7 (PC 11) ← DBF	Call designated Subroutine.	a_{10} a_7	a_9 a_6	a_8 a_5	1 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2				
RET	(SP) ← (SP) 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word.	1	0	0	0	0	0	1	1	2	1				
RETR	(SP) ← (SP) 1 (PC) ← ((SP)) (PSW 4 - 7) ← ((SP))	Return from Subroutine restoring Program Status Word.	1	0	0	1	0	0	1	1	2	1				
Timer/Counter																
EN TCNTI		Enable Internal interrupt Flag for Timer/Counter output.	0	0	1	0	0	1	0	1	1	1				
DIS TCNTI		Disable Internal interrupt Flag for Timer/Counter output.	0	0	1	1	0	1	0	1	1	1				
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator.	0	1	0	0	0	0	1	0	1	1				
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/Counter.	0	1	1	0	0	0	1	0	1	1				
STOP TCNT		Stop Count for Event Counter.	0	1	1	0	0	1	0	1	1	1				
STRT CNT		Start Count for Event Counter.	0	1	0	0	0	1	0	1	1	1				
STRT T		Start Counter for Timer.	0	1	0	1	0	1	0	1	1	1				
Miscellaneous																
NOP		No Operation performed.	0	0	0	0	0	0	0	0	1	1				

Notes:

1 Instruction Code Designations r and p form the binary representation of the Registers and Ports involved.
2 The dot under the appropriate flag bit indicates that its content is subject to change by the instruction it appears in.
3 References to the address and data are specified in bytes 2 and/or 1 of the instruction.
4 Numerical Subscripts appearing in the FUNCTION column reference the specific bits affected.

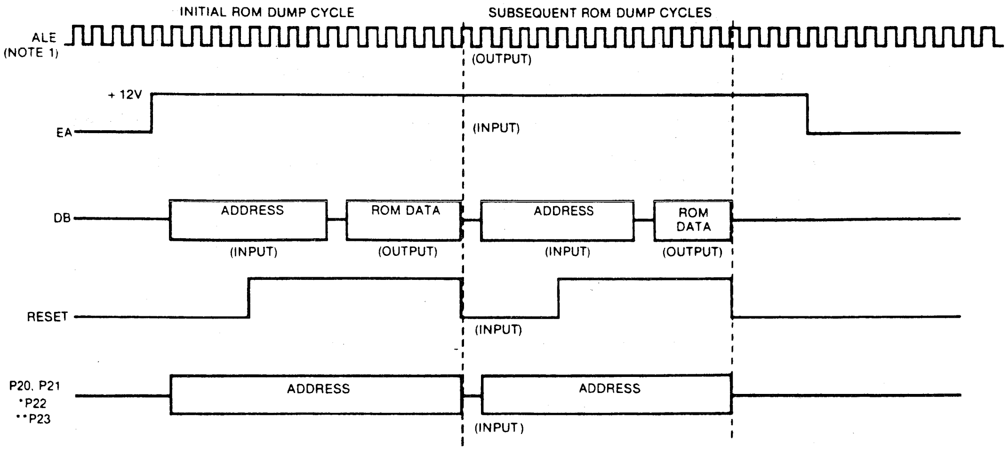
Symbol Definitions:

SYMBOL	DESCRIPTION
A	The Accumulator
AC	The Auxiliary Carry Flag
addr	Program Memory Address (12 bits)
Bb	Bit Designator (b = 0 – 7)
BS	The Bank Switch
BUS	The BUS Port
C	Carry Flag
CLK	Clock Signal
CNT	Event Counter
D	Nibble Designator (4 bits)
data	Number or Expression (8 bits)
DBF	Memory Bank Flip-Flop
F_0, F_1	Flags 0, 1
I	Interrupt
P	"In-Page" Operation Designator

SYMBOL	DESCRIPTION
P_p	Port Designator (p = 1, 2 or 4 – 7)
PSW	Program Status Word
Rr	Register Designator (r = 0, 1 or 0 – 7)
SP	Stack Pointer
T	Timer
TF	Timer Flag
T_0, T_1	Testable Flags 0, 1
X	External RAM
=	Prefix for Immediate Data
@	Prefix for Indirect Address
S	Program Counter's Current Value
(x)	Contents of External RAM Location
((x))	Contents of Memory Location Addressed by the Contents of External RAM Location
←	Replaced By

5

SUGGESTED ROM VERIFICATION ALGORITHM FOR H-MOS DEVICES ONLY



P22 = 0V (8048H)

P23 = 0V (8048H/8049H)

*8049H/8050AH

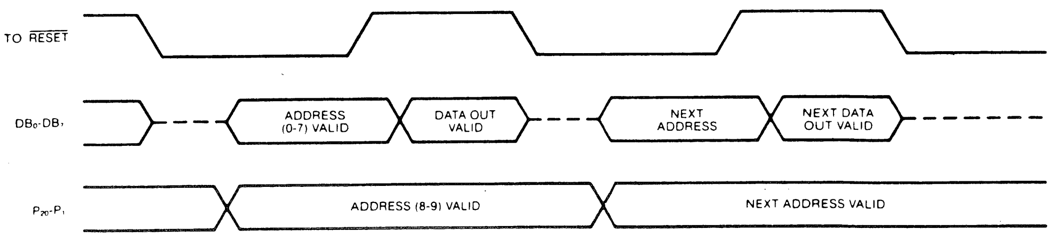
**8050AH

VCC = VDD = + 5V

VSS = 0V

NOTE 1: ALE IS FUNCTION OF X1, X2 INPUTS. PLEASE REFER TO FIGURE ON PAGE 10-20 FOR OSCILLATOR CONFIGURATIONS

VERIFY MODE (ROM/EPROM)



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ORDERING INFORMATION

MHS PART NUMBER	TEMPERATURE RANGE	FREQUENCY (MHz)	V_{CC} (Volts)	PACKAGE
D - 8048 H	COMMERCIAL (0° C + 70° C)	8	5 ± 10 %	CERDIP
P - 8048 H	"	"	"	PLASTIC
D - 8035 HL	"	"	"	CERDIP
P - 8035 HL	"	"	"	PLASTIC
D - 8048 H - 1	COMMERCIAL (0° C + 70° C)	11	5 ± 10 %	CERDIP
P - 8048 H - 1	"	"	"	PLASTIC
D - 8035 HL - 1	"	"	"	CERDIP
P - 8035 HL - 1	"	"	"	PLASTIC

5

PIN DESCRIPTION

Designation	Pin =	Function
V_{SS}	20	Circuit GND potential
V_{DD}	26	Low power standby pin +5V during normal operation
V_{CC}	40	Main power supply; +5V during operation.
PROG	25	Output strobe for 8243 I/O expander.
P10-P17 Port 1	27-34	8-bit quasi-bidirectional port.
P20-27 Port 2	21-24 35-38	8-bit quasi-bidirectional port. P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243 or 82C43.
DB0-DB7 BUS	12-19	True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.
TO	1	Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction.
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.
$\overline{INT}$	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low)(at least 3 machine cycles)
$\overline{RD}$	8	Output strobe activated during a BUS read. Can be used to enable data onto the bus from an external device. Used as a read strobe to external data memory. (Active low)
$\overline{RESET}$	4	Input which is used to initialize the processor. (Active low) (Non TTL V_{IH}) Used during ROM verification and power down
$\overline{WR}$	10	Output strobe during a bus write. (Active low) Used as write strobe to external data memory.
ALE	11	Address latch enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.
$\overline{PSEN}$	9	Program store enable. This output occurs only during a fetch to external program memory. (Active low)
$\overline{SS}$	5	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction. (Active low)
EA	7	External access input which forces all program memory fetches to reference external memory. Useful for emulation and debug (Active high), and essential for testing and program verification (+12V).
XTAL1	2	One side of crystal input for internal oscillator. Also input for external source. (Non TTL V_{IH})
XTAL2	3	Other side of crystal input.

MATRA-HARRIS SEMICONDUCTEURS

data sheet

8086
16-BIT HMOS MICROPROCESSOR

- **Direct Addressing Capability to 1 MByte of Memory**
- **Architecture Designed for Powerful Assembly Language and Efficient High Level Languages.**
- **14 Word, by 16-Bit Register Set with Symmetrical Operations**
- **24 Operand Addressing Modes**
- **Bit, Byte, Word, and Block Operations**
- **8 and 16-Bit Signed and Unsigned Arithmetic in Binary or Decimal Including Multiply and Divide**
- **Range of Clock Rates:**
  5 MHz for 8086,
  8 MHz for 8086-2
  10 MHz for 8086-1
- **MULTIBUS™ System Compatible Interface**

The MHS 8086 high performance 16-bit CPU is available in three clock rates : 5, 8 and 10 MHz. The CPU is implemented in N-Channel, depletion load, silicon gate technology (HMOS), and packaged in a 40-pin CerDIP package. The 8086 operates in both single processor and multiple processor configurations to achieve high performance levels.

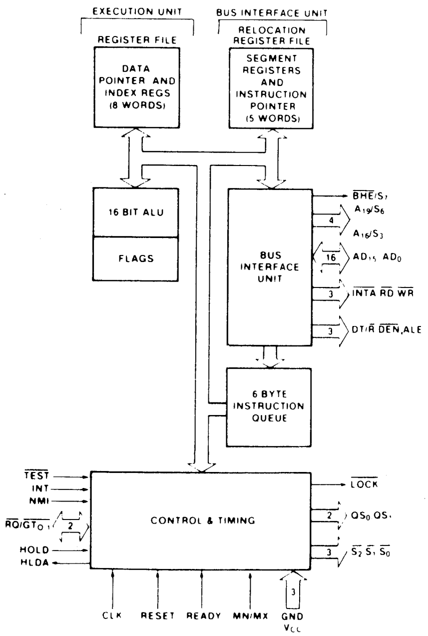

Figure 1. 8086 CPU Block Diagram

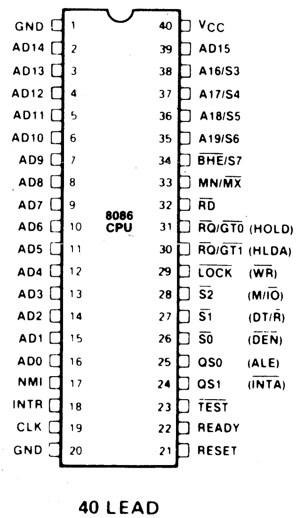

Figure 2. 8086 Pin Configuration

Table 1. Pin Description

The following pin function descriptions are for 8086 systems in either minimum or maximum mode. The "Local Bus" in these descriptions is the direct multiplexed bus interface connection to the 8086 (without regard to additional bus buffers).

<table>
<tr><th>Symbol</th><th>Pin No.</th><th>Type</th><th>Name and Function</th></tr>
<tr><td>AD_{15}-AD_0</td><td>2-16, 39</td><td>I/O</td><td>Address Data Bus: These lines constitute the time multiplexed memory/IO address (T_1) and data (T_2, T_3, T_W, T_4) bus. A_0 is analogous to $\overline{BHE}$ for the lower byte of the data bus, pins D_7-D_0. It is LOW during T_1 when a byte is to be transferred on the lower portion of the bus in memory or I/O operations. Eight-bit oriented devices tied to the lower half would normally use A_0 to condition chip select functions. (See $\overline{BHE}$.) These lines are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge."</td></tr>
<tr><td>A_{19}/S_6,
A_{18}/S_5,
A_{17}/S_4,
A_{16}/S_3</td><td>35-38</td><td>O</td><td>Address/Status: During T_1 these are the four most significant address lines for memory operations. During I/O operations these lines are LOW. During memory and I/O operations, status information is available on these lines during T_2, T_3, T_W, and T_4. The status of the interrupt enable FLAG bit (S_5) is updated at the beginning of each CLK cycle. A_{17}/S_4 and A_{16}/S_3 are encoded as shown.

This information indicates which relocation register is presently being used for data accessing.

These lines float to 3-state OFF during local bus "hold acknowledge."

<table>
<tr><th>A_{17}/S_4</th><th>A_{16}/S_3</th><th>Characteristics</th></tr>
<tr><td>0 (LOW)</td><td>0</td><td>Alternate Data</td></tr>
<tr><td>0</td><td>1</td><td>Stack</td></tr>
<tr><td>1 (HIGH)</td><td>0</td><td>Code or None</td></tr>
<tr><td>1</td><td>1</td><td>Data</td></tr>
<tr><td>S_6 is 0 (LOW)</td><td></td><td></td></tr>
</table></td></tr>
<tr><td>$\overline{BHE}/S_7$</td><td>34</td><td>O</td><td>Bus High Enable/Status: During T_1 the bus high enable signal ($\overline{BHE}$) should be used to enable data onto the most significant half of the data bus, pins D_{15}-D_8. Eight-bit oriented devices tied to the upper half of the bus would normally use $\overline{BHE}$ to condition chip select functions. $\overline{BHE}$ is LOW during T_1 for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the high portion of the bus. The S_7 status information is available during T_2, T_3, and T_4. The signal is active LOW, and floats to 3-state OFF in "hold." It is LOW during T_1 for the first interrupt acknowledge cycle.

<table>
<tr><th>$\overline{BHE}$</th><th>A_0</th><th>Characteristics</th></tr>
<tr><td>0</td><td>0</td><td>Whole word</td></tr>
<tr><td>0</td><td>1</td><td>Upper byte from/ to odd address</td></tr>
<tr><td>1</td><td>0</td><td>Lower byte from/ to even address</td></tr>
<tr><td>1</td><td>1</td><td>None</td></tr>
</table></td></tr>
<tr><td>$\overline{RD}$</td><td>32</td><td>O</td><td>Read: Read strobe indicates that the processor is performing a memory of I/O read cycle, depending on the state of the S_2 pin. This signal is used to read devices which reside on the 8086 local bus. $\overline{RD}$ is active LOW during T_2, T_3 and T_W of any read cycle, and is guaranteed to remain HIGH in T_2 until the 8086 local bus has floated.

This signal floats to 3-state OFF in "hold acknowledge."</td></tr>
<tr><td>READY</td><td>22</td><td>I</td><td>READY: is the acknowledgement from the addressed memory or I/O device that it will complete the data transfer. The READY signal from memory/IO is synchronized by the 8284A Clock Generator to form READY. This signal is active HIGH. The 8086 READY input is not synchronized. Correct operation is not guaranteed if the setup and hold times are not met.</td></tr>
<tr><td>INTR</td><td>18</td><td>I</td><td>Interrupt Request: is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.</td></tr>
<tr><td>$\overline{TEST}$</td><td>23</td><td>I</td><td>$\overline{TEST}$: input is examined by the "Wait" instruction. If the $\overline{TEST}$ input is LOW execution continues, otherwise the processor waits in an "Idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.</td></tr>
</table>

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Table 1. Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
NMI	17	I	**Non-maskable interrupt:** an edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from a LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.
RESET	21	I	**Reset:** causes the processor to immediately terminate its present activity. The signal must be active HIGH for at least four clock cycles. It restarts execution, as described in the Instruction Set description, when RESET returns LOW. RESET is internally synchronized.
CLK	19	I	**Clock:** provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.
V_{CC}	40		V_{CC}: +5V power supply pin.
GND	1, 20		**Ground**
MN/$\overline{MX}$	33	I	**Minimum/Maximum:** indicates what mode the processor is to operate in. The two modes are discussed in the following sections.

The following pin function descriptions are for the 8086/8288 system in maximum mode (i.e., MN/$\overline{MX}$ = V_{SS}). Only the pin functions which are unique to maximum mode are described; all other pin functions are as described above.

<table>
<tr><td>$\overline{S_2}$, $\overline{S_1}$, $\overline{S_0}$</td><td>26-28</td><td>O</td><td>Status: active during T_4, T_1, and T_2 and is returned to the passive state (1,1,1) during T_3 or during T_W when READY is HIGH. This status is used by the 8288 Bus Controller to generate all memory and I/O access control signals. Any change by $\overline{S_2}$, $\overline{S_1}$, or $\overline{S_0}$ during T_4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T_3 or T_W is used to indicate the end of a bus cycle.

These signals float to 3-state OFF in "hold acknowledge." These status lines are encoded as shown.

<table>
<tr><th>$\overline{S_2}$</th><th>$\overline{S_1}$</th><th>$\overline{S_0}$</th><th>Characteristics</th></tr>
<tr><td>0 (LOW)</td><td>0</td><td>0</td><td>Interrupt Acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read I/O Port</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write I/O Port</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Halt</td></tr>
<tr><td>1 (HIGH)</td><td>0</td><td>0</td><td>Code Access</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read Memory</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write Memory</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Passive</td></tr>
</table></td></tr>
<tr><td>$\overline{RQ}/\overline{GT}_0$,
$\overline{RQ}/\overline{GT}_1$</td><td>30, 31</td><td>I/O</td><td>Request/Grant: pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bidirectional with $\overline{RQ}/\overline{GT}_0$ having higher priority than $\overline{RQ}/\overline{GT}_1$. $\overline{RQ}/\overline{GT}$ has an internal pull-up resistor so may be left unconnected. The request/grant sequence is as follows (see Figure 9):

1. A pulse of 1 CLK wide from another local bus master indicates a local bus request ("hold") to the 8086 (pulse 1).
2. During a T_4 or T_I clock cycle, a pulse 1 CLK wide from the 8086 to the requesting master (pulse 2), indicates that the 8086 has allowed the local bus to float and that it will enter the "hold acknowledge" state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "hold acknowledge."
3. A pulse 1 CLK wide from the requesting master indicates to the 8086 (pulse 3) that the "hold" request is about to end and that the 8086 can reclaim the local bus at the next CLK.

Each master-master exchange of the local bus is a sequence of 3 pulses. There must be one dead CLK cycle after each bus exchange. Pulses are active LOW.

If the request is made while the CPU is performing a memory cycle, it will release the local bus during T_4 of the cycle when all the following conditions are met:

1. Request occurs on or before T_2.
2. Current cycle is not the low byte of a word (on an odd address).
3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence.
4. A locked instruction is not currently executing.</td></tr>
</table>

Table 1. Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
			If the local bus is idle when the request is made the two possible events will follow: 1. Local bus will be released during the next clock. 2. A memory cycle will start within 3 clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied.
$\overline{\text{LOCK}}$	29	O	**$\overline{\text{LOCK}}$:** output indicates that other system bus masters are not to gain control of the system bus while $\overline{\text{LOCK}}$ is active LOW. The $\overline{\text{LOCK}}$ signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and floats to 3-state OFF in "hold acknowledge."
QS_1, QS_0	24, 25	O	**Queue Status:** The queue status is valid during the CLK cycle after which the queue operation is performed. QS_1 and QS_0 provide status to allow external tracking of the internal 8086 instruction queue.

The following pin function descriptions are for the 8086 in minimum mode (i.e., $MN/\overline{MX} = V_{CC}$). Only the pin functions which are unique to minimum mode are described; all other pin functions are as described above.

$M/\overline{IO}$	28	O	**Status line:** logically equivalent to S_2 in the maximum mode. It is used to distinguish a memory access from an I/O access. $M/\overline{IO}$ becomes valid in the T_4 preceding a bus cycle and remains valid until the final T_4 of the cycle (M = HIGH, IO = LOW). $M/\overline{IO}$ floats to 3-state OFF in local bus "hold acknowledge."
$\overline{\text{WR}}$	29	O	**Write:** indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the $M/\overline{IO}$ signal. $\overline{\text{WR}}$ is active for T_2, T_3 and T_W of any write cycle. It is active LOW, and floats to 3-state OFF in local bus "hold acknowledge."
$\overline{\text{INTA}}$	24	O	**$\overline{\text{INTA}}$** is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T_2, T_3 and T_W of each interrupt acknowledge cycle.
ALE	25	O	**Address Latch Enable:** provided by the processor to latch the address into the 8282/8283 address latch. It is a HIGH pulse active during T_1 of any bus cycle. Note that ALE is never floated.
$DT/\overline{R}$	27	O	**Data Transmit/Receive:** needed in minimum system that desires to use an 8286/8287 data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically $DT/\overline{R}$ is equivalent to $\overline{S_1}$ in the maximum mode, and its timing is the same as for $M/\overline{IO}$. (T = HIGH, R = LOW.) This signal floats to 3-state OFF in local bus "hold acknowledge."
$\overline{\text{DEN}}$	26	O	**Data Enable:** provided as an output enable for the 8286/8287 in a minimum system which uses the transceiver. $\overline{\text{DEN}}$ is active LOW during each memory and I/O access and for INTA cycles. For a read or $\overline{\text{INTA}}$ cycle it is active from the middle of T_2 until the middle of T_4, while for a write cycle it is active from the beginning of T_2 until the middle of T_4. $\overline{\text{DEN}}$ floats to 3-state OFF in local bus "hold acknowledge."
HOLD, HLDA	31, 30	I/O	**HOLD:** indicates that another master is requesting a local bus "hold." To be acknowledged, HOLD must be active HIGH. The processor receiving the "hold" request will issue HLDA (HIGH) as an acknowledgement in the middle of a T_4 or T_I clock cycle. Simultaneous with the issuance of HLDA the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor will LOWer HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. The same rules as for $\overline{\text{RQ}}/\overline{\text{GT}}$ apply regarding when the local bus will be released. HOLD is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the setup time.

FUNCTIONAL DESCRIPTION

GENERAL OPERATION

The internal functions of the 8086 processor are partitioned logically into two processing units. The first is the Bus Interface Unit (BIU) and the second is the Execution Unit (EU) as shown in the block diagram of Figure 1.

These units can interact directly but for the most part perform as separate asynchronous operational processors. The bus interface unit provides the functions related to instruction fetching and queuing, operand fetch and store, and address relocation. This unit also provides the basic bus control. The overlap of instruction pre-fetching provided by this unit serves to increase processor performance through improved bus bandwidth utilization. Up to 6 bytes of the instruction stream can be queued while waiting for decoding and execution.

The instruction stream queuing mechanism allows the BIU to keep the memory utilized very efficiently. Whenever there is space for at least 2 bytes in the queue, the BIU will attempt a word fetch memory cycle. This greatly reduces "dead time" on the memory bus. The queue acts as a First-In-First-Out (FIFO) buffer, from which the EU extracts instruction bytes as required. If the queue is empty (following a branch instruction, for example), the first byte into the queue immediately becomes available to the EU.

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The execution unit receives pre-fetched instructions from the BIU queue and provides un-relocated operand addresses to the BIU. Memory operands are passed through the BIU for processing by the EU, which passes results to the BIU for storage. See the Instruction Set description for further register set and architectural descriptions.

MEMORY ORGANIZATION

The processor provides a 20-bit address to memory which locates the byte being referenced. The memory is organized as a linear array of up to 1 million bytes, addressed as 00000(H) to FFFFF(H). The memory is logically divided into code, data, extra data, and stack segments of up to 64K bytes each, with each segment falling on 16-byte boundaries. (See Figure 3a.)

All memory references are made relative to base addresses contained in high speed segment registers. The segment types were chosen based on the addressing needs of programs. The segment register to be selected is automatically chosen according to the rules of the following table. All information in one segment type share the same logical attributes (e.g. code or data). By structuring memory into relocatable areas of similar characteristics and by automatically selecting segment registers, programs are shorter, faster, and more structured.

Word (16-bit) operands can be located on even or odd address boundaries and are thus not constrained to even boundaries as is the case in many 16-bit computers. For address and data operands, the least significant byte of the word is stored in the lower valued address location and the most significant byte in the next higher address location. The BIU automatically performs the proper number of memory accesses, one if the word operand is on an even byte boundary and two if it is on an odd byte boundary. Except for the performance penalty, this double access is transparent to the software. This performance penalty does not occur for instruction fetches, only word operands.

Physically, the memory is organized as a high bank (D_{15}-D_8) and a low bank (D_7-D_0) of 512K 8-bit bytes addressed in parallel by the processor's address lines

A_{19} - A_1. Byte data with even addresses is transferred on the D_7-D_0 bus lines while odd addressed byte data (A_0 HIGH) is transferred on the D_{15}-D_8 bus lines. The processor provides two enable signals, $\overline{BHE}$ and A_0, to selectively allow reading from or writing into either an odd byte location, even byte location, or both. The instruction stream is fetched from memory as words and is addressed internally by the processor to the byte level as necessary.

Memory Reference Need	Segment Register Used	Segment Selection Rule
Instructions	CODE (CS)	Automatic with all instruction prefetch.
Stack	STACK (SS)	All stack pushes and pops. Memory references relative to BP base register except data references.
Local Data	DATA (DS)	Data references when: relative to stack, destination of string operation, or explicitly overridden.
External (Global) Data	EXTRA (ES)	Destination of string operations: Explicitly selected using a segment override.

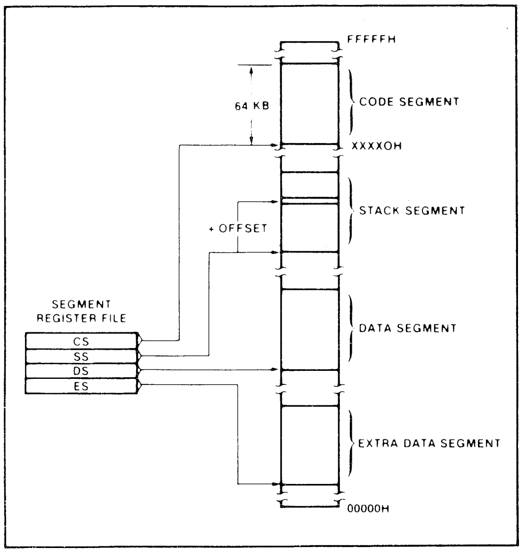

Figure 3a. Memory Organization

In referencing word data the BIU requires one or two memory cycles depending on whether or not the starting byte of the word is on an even or odd address, respectively. Consequently, in referencing word operands performance can be optimized by locating data on even address boundaries. This is an especially useful technique for using the stack, since odd address references to the stack may adversely affect the context switching time for interrupt processing or task multiplexing.

Certain locations in memory are reserved for specific CPU operations (see Figure 3b.) Locations from address FFFF0H through FFFFFH are reserved for operations including a jump to the initial program loading routine. Following RESET, the CPU will always begin execution at location FFFF0H where the jump must be. Locations 00000H through 003FFH are reserved for interrupt operations. Each of the 256 possible interrupt types has its service routine pointed to by a 4-byte pointer element consisting of a 16-bit segment address and a 16-bit offset address. The pointer elements are assumed to have been stored at the respective places in reserved memory prior to occurrence of interrupts.

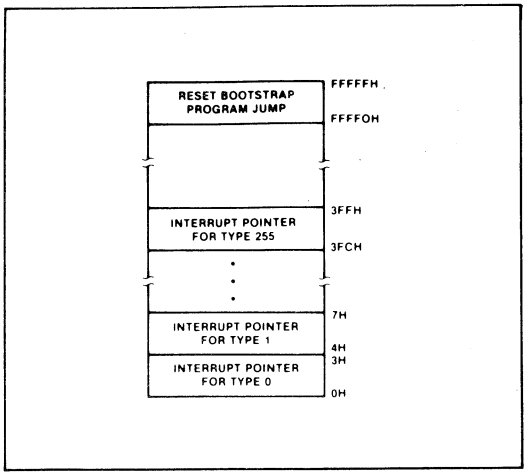

Figure 3b. Reserved Memory Locations

MINIMUM AND MAXIMUM MODES

The requirements for supporting minimum and maximum 8086 systems are sufficiently different that they cannot be done efficiently with 40 uniquely defined pins. Consequently, the 8086 is equipped with a strap pin (MN/$\overline{MX}$) which defines the system configuration. The definition of a certain subset of the pins changes dependent on the condition of the strap pin. When MN/$\overline{MX}$ pin is strapped to GND, the 8086 treats pins 24 through 31 in maximum mode. An 8288 bus controller interprets status information coded into $\overline{S_0}$,$\overline{S_1}$,$\overline{S_2}$ to generate bus timing and control signals compatible with the MULTIBUS™ architecture. When the MN/$\overline{MX}$ pin is strapped to V_{CC}, the 8086 generates bus control signals itself on pins 24 through 31, as shown in parentheses in Figure 2. Examples of minimum mode and maximum mode systems are shown in Figure 4.

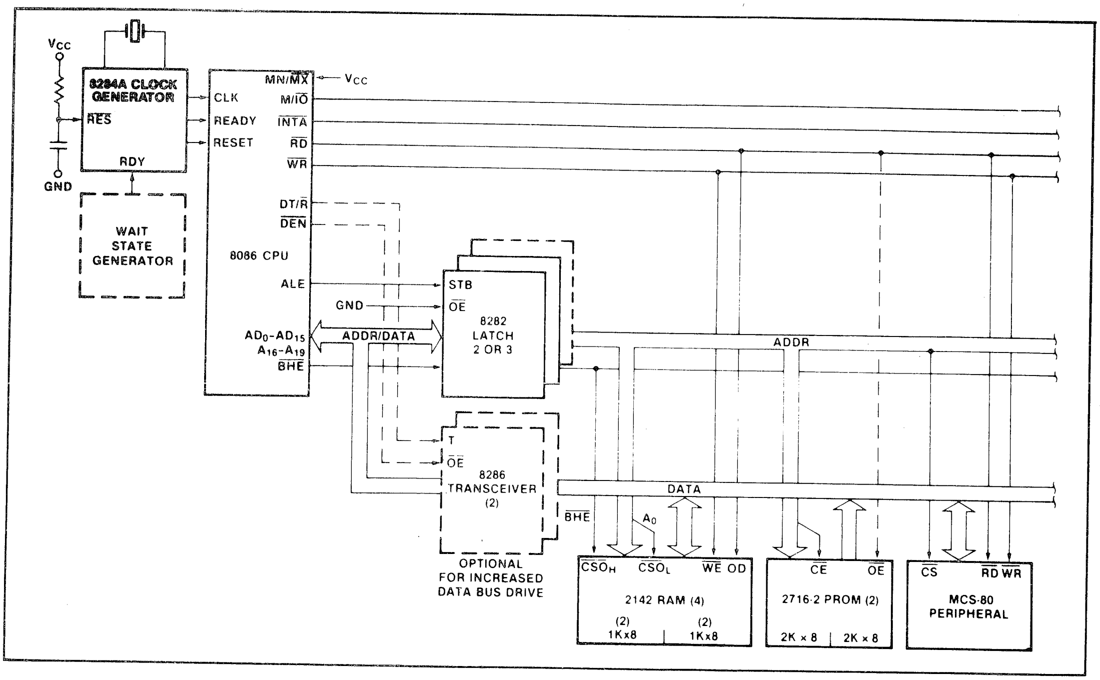

Figure 4a. Minimum Mode 8086 Typical Configuration

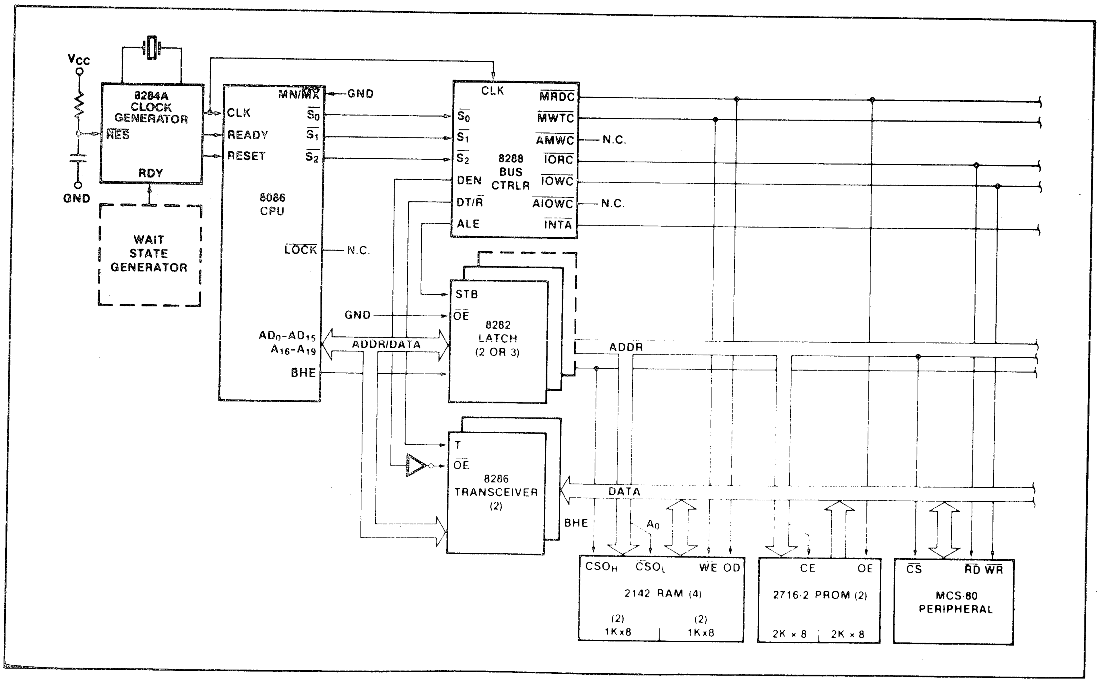

Figure 4b. Maximum Mode 8086 Typical Configuration

BUS OPERATION

The 8086 has a combined address and data bus commonly referred to as a time multiplexed bus. This technique provides the most efficient use of pins on the processor while permitting the use of a standard 40-lead package. This "local bus" can be buffered directly and used throughout the system with address latching provided on memory and I/O modules. In addition, the bus can also be demultiplexed at the processor with a single set of address latches if a standard non-multiplexed bus is desired for the system.

Each processor bus cycle consists of at least four CLK cycles. These are referred to as T_1, T_2, T_3 and T_4 (see Figure 5). The address is emitted from the processor during T_1 and data transfer occurs on the bus during T_3 and T_4. T_2 is used primarily for changing the direction of the bus during read operations. In the event that a "NOT READY" indication is given by the addressed device, "Wait" states (T_W) are inserted between T_3 and T_4. Each inserted "Wait" state is of the same duration as a CLK cycle. Periods can occur between 8086 bus cycles. These are referred to as "Idle" states (T_I) or inactive CLK cycles. The processor uses these cycles for internal housekeeping.

During T_1 of any bus cycle the ALE (Address Latch Enable) signal is emitted (by either the processor or the 8288 bus controller, depending on the MN/$\overline{MX}$ strap). At the trailing edge of this pulse, a valid address and certain status information for the cycle may be latched.

Status bits $\overline{S_0}$, $\overline{S_1}$, and $\overline{S_2}$ are used, in maximum mode, by the bus controller to identify the type of bus transaction according to the following table:

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	CHARACTERISTICS
0 (LOW)	0	0	Interrupt Acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1 (HIGH)	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

Status bits S_3 through S_7 are multiplexed with high-order address bits and the $\overline{BHE}$ signal, and are therefore valid during T_2 through T_4. S_3 and S_4 indicate which segment register (see Instruction Set description) was used for this bus cycle in forming the address, according to the following table:

S_4	S_3	CHARACTERISTICS
0 (LOW)	0	Alternate Data (extra segment)
0	1	Stack
1 (HIGH)	0	Code or None
1	1	Data

S_5 is a reflection of the PSW interrupt enable bit. S_6=0 and S_7 is a spare status bit.

I/O ADDRESSING

In the 8086, I/O operations can address up to a maximum of 64K I/O byte registers or 32K I/O word registers. The I/O address appears in the same format as the memory address on bus lines A_{15}-A_0. The address lines A_{19}-A_{16} are zero in I/O operations. The variable I/O instructions which use register DX as a pointer have full address capability while the direct I/O instructions directly address one or two of the 256 I/O byte locations in page 0 of the I/O address space.

I/O ports are addressed in the same manner as memory locations. Even addressed bytes are transferred on the D_7-D_0 bus lines and odd addressed bytes on D_{15}-D_8. Care must be taken to assure that each register within an 8-bit peripheral located on the lower portion of the bus be addressed as even.

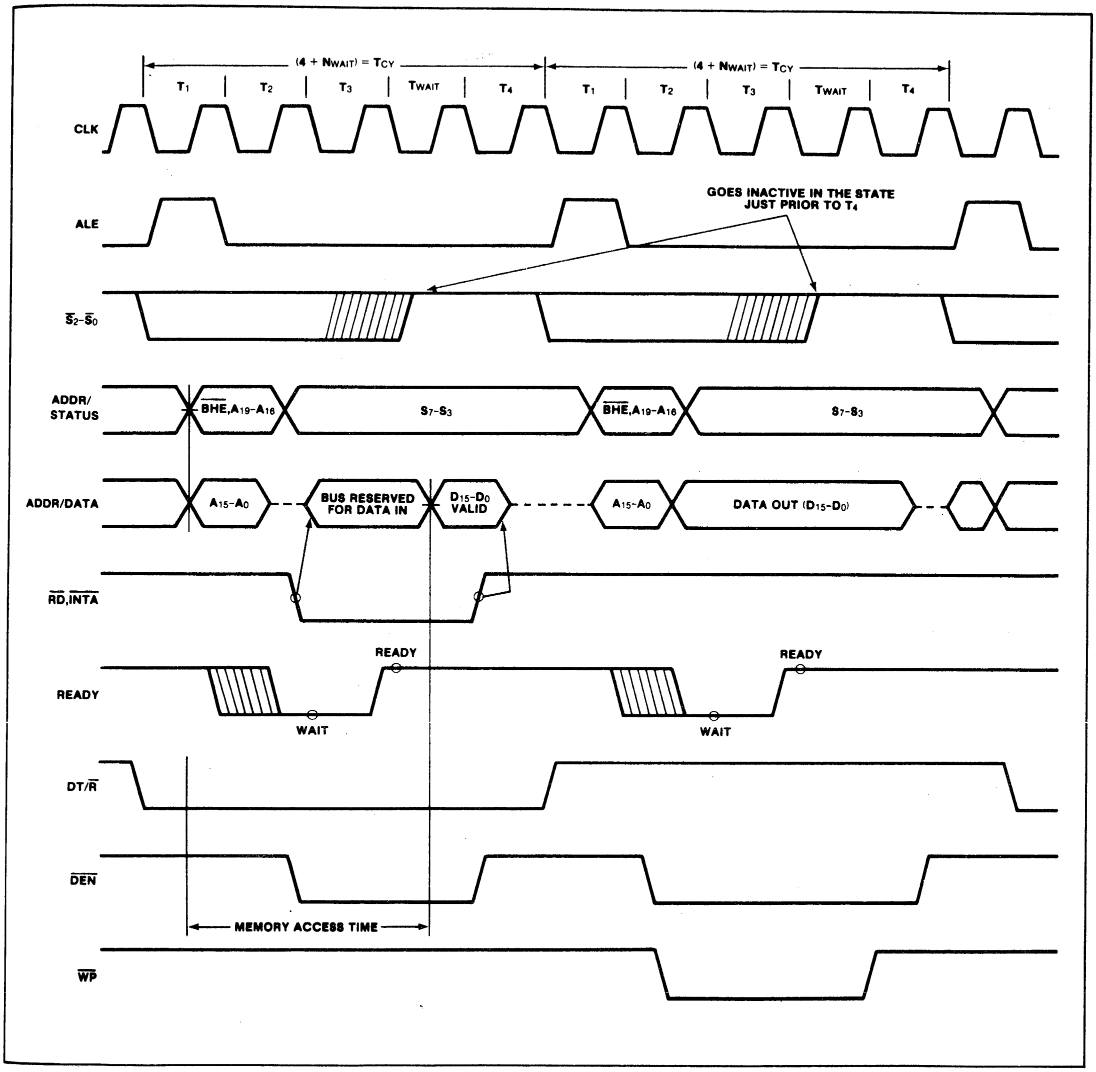

Figure 5. Basic System Timing

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EXTERNAL INTERFACE

PROCESSOR RESET AND INITIALIZATION

Processor initialization or start up is accomplished with activation (HIGH) of the RESET pin. The 8086 RESET is required to be HIGH for greater than 4 CLK cycles. The 8086 will terminate operations on the high-going edge of RESET and will remain dormant as long as RESET is HIGH. The low-going transition of RESET triggers an internal reset sequence for approximately 10 CLK cycles. After this interval the 8086 operates normally beginning with the instruction in absolute location FFFF0H (see Figure 3B). The details of this operation are specified in the Instruction Set description of the MCS-86 Family User's Manual. The RESET input is internally synchronized to the processor clock. At initialization the HIGH-to-LOW transition of RESET must occur no sooner than 50 μs after power-up, to allow complete initialization of the 8086.

NMI may not be asserted prior to the 2nd CLK cycle following the end of RESET.

INTERRUPT OPERATIONS

Interrupt operations fall into two classes; software or hardware initiated. The software initiated interrupts and software aspects of hardware interrupts are specified in the Instruction Set description. Hardware interrupts can be classified as non-maskable or maskable.

Interrupts result in a transfer of control to a new program location. A 256-element table containing address pointers to the interrupt service program locations resides in absolute locations 0 through 3FFH (see Figure 3b), which are reserved for this purpose. Each element in the table is 4 bytes in size and corresponds to an interrupt "type". An interrupting device supplies an 8-bit type number, during the interrupt acknowledge sequence, which is used to "vector" through the appropriate element to the new interrupt service program location.

NON-MASKABLE INTERRUPT (NMI)

The processor provides a single non-maskable interrupt pin (NMI) which has higher priority than the maskable interrupt request pin (INTR). A typical use would be to activate a power failure routine. The NMI is edge-triggered on a LOW-to-HIGH transition. The activation of this pin causes a type 2 interrupt. (See Instruction Set description.)

NMI is required to have a duration in the HIGH state of greater than two CLK cycles, but is not required to be synchronized to the clock. Any high-going transition of NMI is latched on-chip and will be serviced at the end of the current instruction or between whole moves of a block-type instruction. Worst case response to NMI would be for multiply, divide, and variable shift instructions. There is no specification on the occurrence of the low-going edge; it may occur before, during, or after the servicing of NMI. Another high-going edge triggers another response if it occurs after the start of the NMI procedure. The signal must be free of logical spikes in general and be free of bounces on the low-going edge to avoid triggering extraneous responses.

MASKABLE INTERRUPT (INTR)

The 8086 provides a single interrupt request input (INTR) which can be masked internally by software with the resetting of the interrupt enable FLAG status bit. The interrupt request signal is level triggered. It is internally synchronized during each clock cycle on the high-going edge of CLK. To be responded to, INTR must be present (HIGH) during the clock period preceding the end of the current instruction or the end of a whole move for a block-type instruction. During the interrupt response sequence further interrupts are disabled. The enable bit is reset as part of the response to any interrupt (INTR, NMI, software interrupt or single-step), although the

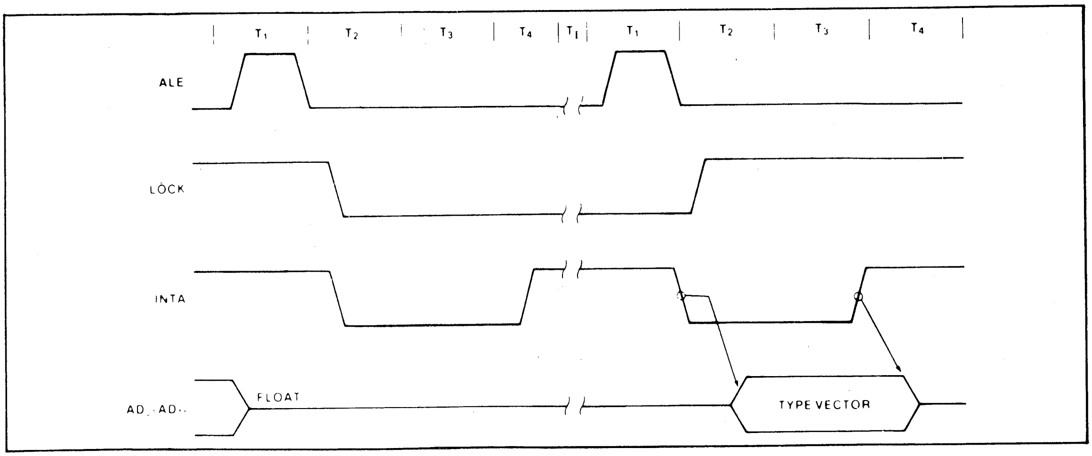


Figure 6. Interrupt Acknowledge Sequence

FLAGS register which is automatically pushed onto the stack reflects the state of the processor prior to the interrupt. Until the old FLAGS register is restored the enable bit will be zero unless specifically set by an instruction.

During the response sequence (figure 6) the processor executes two successive (back-to-back) interrupt acknowledge cycles. The 8086 emits the LOCK signal from T_2 of the first bus cycle until T_2 of the second. A local bus "hold" request will not be honored until the end of the second bus cycle. In the second bus cycle a byte is fetched from the external interrupt system (e.g., 8259A PIC) which identifies the source (type) of the interrupt. This byte is multiplied by four and used as a pointer into the interrupt vector lookup table. An INTR signal left HIGH will be continually responded to within the limitations of the enable bit and sample period. The INTERRUPT RETURN instruction includes a FLAGS pop which returns the status of the original interrupt enable bit when it restores the FLAGS.

HALT

When a software "HALT" instruction is executed the processor indicates that it is entering the "HALT" state in one of two ways depending upon which mode is strapped. In minimum mode, the processor issues one ALE with no qualifying bus control signals. In Maximum Mode, the processor issues appropriate HALT status on $\overline{S_2}\overline{S_1}\overline{S_0}$ and the 8288 bus controller issues one ALE. The 8086 will not leave the "HALT" state when a local bus "hold" is entered while in "HALT". In this case, the processor reissues the HALT indicator. An interrupt request or RESET will force the 8086 out of the "HALT" state.

READ/MODIFY/WRITE (SEMAPHORE) OPERATIONS VIA LOCK

The $\overline{LOCK}$ status information is provided by the processor when directly consecutive bus cycles are required during the execution of an instruction. This provides the processor with the capability of performing read/modify/write operations on memory (via the Exchange Register With Memory instruction, for example) without the possibility of another system bus master receiving intervening memory cycles. This is useful in multiprocessor system configurations to accomplish "test and set lock" operations. The $\overline{LOCK}$ signal is activated (forced LOW) in the clock cycle following the one in which the software "LOCK" prefix instruction is decoded by the EU. It is deactivated at the end of the last bus cycle of the instruction following the "LOCK" prefix instruction. While $\overline{LOCK}$ is active a request on a RQ/GT pin will be recorded and then honored at the end of the LOCK.

EXTERNAL SYNCHRONIZATION VIA TEST

As an alternative to the interrupts and general I/O capabilities, the 8086 provides a single software-testable input known as the $\overline{TEST}$ signal. At any time the program may execute a WAIT instruction. If at that time the $\overline{TEST}$ signal is inactive (HIGH), program execution becomes suspended while the processor waits for $\overline{TEST}$ to become active. It must remain active for at least 5 CLK cycles. The WAIT instruction is re-executed repeatedly until that time. This activity does not consume bus cycles. The processor remains in an idle state while waiting. All 8086 drivers go to 3-state OFF if bus "Hold" is entered. If interrupts are enabled, they may occur while the processor is waiting. When this occurs the processor fetches the WAIT instruction one extra time, processes the interrupt, and then re-fetches and re-executes the WAIT instruction upon returning from the interrupt.

BASIC SYSTEM TIMING

Typical system configurations for the processor operating in minimum mode and in maximum mode are shown in Figures 4a and 4b, respectively. In minimum mode, the MN/$\overline{MX}$ pin is strapped to V_{CC} and the processor emits bus control signals in a manner similar to the 8085. In maximum mode, the MN/$\overline{MX}$ pin is strapped to V_{SS} and the processor emits coded status information which the 8288 bus controller uses to generate MULTIBUS compatible bus control signals. Figure 5 illustrates the signal timing relationships.

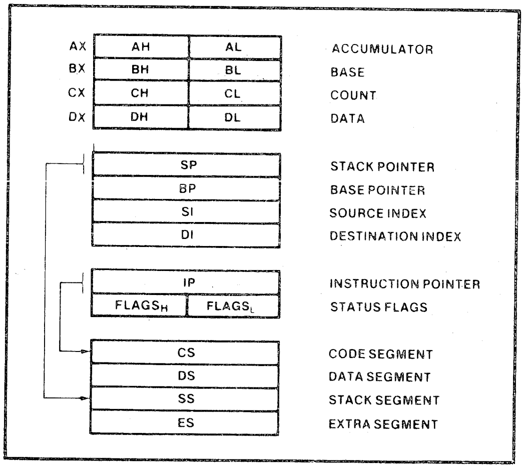


Figure 7. 8086 Register Model

SYSTEM TIMING — MINIMUM SYSTEM

The read cycle begins in T_1 with the assertion of the Address Latch Enable (ALE) signal. The trailing (low-going) edge of this signal is used to latch the address information, which is valid on the local bus at this time, into the 8282/8283 latch. The $\overline{BHE}$ and A_0 signals address the low, high, or both bytes. From T_1 to T_4 the M/$\overline{IO}$ signal indicates a memory or I/O operation. At T_2 the address is removed from the local bus and the bus goes to a high impedance state. The read control signal is also asserted at T_2. The read ($\overline{RD}$) signal causes the addressed device to enable its data bus drivers to the local bus. Some time later valid data will be available on the bus and the addressed device will drive the READY line HIGH. When the processor returns the read signal to a HIGH level, the addressed device will again 3-state its bus drivers. If a transceiver (8286/8287) is required to buffer the 8086 local bus, signals DT/$\overline{R}$ and $\overline{DEN}$ are provided by the 8086.

A write cycle also begins with the assertion of ALE and the emission of the address. The M/$\overline{IO}$ signal is again asserted to indicate a memory or I/O write operation. In the T_2 immediately following the address emission the processor emits the data to be written into the addressed location. This data remains valid until the middle of T_4. During T_2, T_3, and T_W the processor asserts the write control signal. The write ($\overline{WR}$) signal becomes active at the beginning of T_2 as opposed to the read which is delayed somewhat into T_2 to provide time for the bus to float.

The $\overline{BHE}$ and A_0 signals are used to select the proper byte(s) of the memory/IO word to be read or written according to the following table:

$\overline{BHE}$	A0	CHARACTERISTICS
0	0	Whole word
0	1	Upper byte from/ to odd address
1	0	Lower byte from/ to even address
1	1	None

I/O ports are addressed in the same manner as memory location. Even addressed bytes are transferred on the D_7-D_0 bus lines and odd addressed bytes on D_{15}-D_8.

The basic difference between the interrupt acknowledge cycle and a read cycle is that the interrupt acknowledge signal ($\overline{INTA}$) is asserted in place of the read ($\overline{RD}$) signal and the address bus is floated. (See Figure 6.) In the second of two successive INTA cycles, a byte of information is read from bus lines D_7-D_0 as supplied by the interrupt system logic (i.e., 8259A Priority Interrupt Controller). This byte identifies the source (type) of the interrupt. It is multiplied by four and used as a pointer into an interrupt vector lookup table, as described earlier.

BUS TIMING—MEDIUM SIZE SYSTEMS

For medium size systems the MN/$\overline{MX}$ pin is connected to V_{SS} and the 8288 Bus Controller is added to the system as well as an 8282/8283 latch for latching the system address, and a 8286/8287 transceiver to allow for bus loading greater than the 8086 is capable of handling. Signals ALE, DEN, and DT/$\overline{R}$ are generated by the 8288 instead of the processor in this configuration although their timing remains relatively the same. The 8086 status outputs ($\overline{S}_2$, $\overline{S}_1$, and $\overline{S}_0$) provide type-of-cycle information and become 8288 inputs. This bus cycle information specifies read (code, data, or I/O), write (data or I/O), interrupt acknowledge, or software halt. The 8288 thus issues control signals specifying memory read or write, I/O read or write, or interrupt acknowledge. The 8288 provides two types of write strobes, normal and advanced, to be applied as required. The normal write strobes have data valid at the leading edge of write. The advanced write strobes have the same timing as read strobes, and hence data isn't valid at the leading edge of write. The 8286/8287 transceiver receives the usual T and OE inputs from the 8288's DT/$\overline{R}$ and DEN.

The pointer into the interrupt vector table, which is passed during the second INTA cycle, can derive from an 8259A located on either the local bus or the system bus. If the master 8259A Priority Interrupt Controller is positioned on the local bus, a TTL gate is required to disable the 8286/8287 transceiver when reading from the master 8259A during the interrupt acknowledge sequence and software "poll".

D - 8086
ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ....0°C to 70°C
Storage Temperature .... −65°C to +150°C
Voltage on Any Pin with
Respect to Ground .... −1.0 to +7V
Power Dissipation .... 2.5 Watt

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

(8086: T_A = 0°C to 70°C, V_{CC} = 5V ± 10%)
(8086-1: T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)
(8086-2: T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL}=2.5 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
I_{CC}	Power Supply Current: 8086 8086-1 8086-2		340 360 350	mA	T_A = 25°C
I_{LI}	Input Leakage Current		±10	μA	0V ≤ V_{IN} ≤ V_{CC}
I_{LO}	Output Leakage Current		±10	μA	0.45V ≤ V_{OUT} ≤ V_{CC}
V_{CL}	Clock Input Low Voltage	−0.5	+0.6	V	
V_{CH}	Clock Input High Voltage	3.9	V_{CC} + 1.0	V	
C_{IN}	Capacitance of Input Buffer (All input except $AD_0 - AD_{15}$, $\overline{RQ}/\overline{GT}$)		15	pF	fc = 1 MHz
C_{IO}	Capacitance of I/O Buffer ($AD_0 - AD_{15}$, $\overline{RQ}/\overline{GT}$)		15	pF	fc = 1 MHz

A.C. CHARACTERISTICS

(8086 : T_A = 0° C to 70° C, V_{CC} = 5 V ± 10 %)(5 MHz)
(8086-1 : T_A = 0° C to 70° C, V_{CC} = 5 V ± 5 %)(10 MHz)
(8086-2 : T_A = 0° C to 70° C, V_{CC} = 5 V ± 5 %)(8 MHz)

MINIMUM COMPLEXITY SYSTEM TIMING REQUIREMENTS

Symbol	Parameter	5MHz 8086		10MHz 8086-1 (Preliminary)		8MHz 8086-2		Units	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
TCLCL	CLK Cycle Period	200	500	100	500	125	500	ns	
TCLCH	CLK Low Time	118		53		68		ns	
TCHCL	CLK High Time	69		39		44		ns	
TCH1CH2	CLK Rise Time		10		10		10	ns	From 1.0V to 3.5V
TCL2CL1	CLK Fall Time		10		10		10	ns	From 3.5V to 1.0V
TDVCL	Data in Setup Time	30		5		20		ns	
TCLDX	Data in Hold Time	10		10		10		ns	
TR1VCL	RDY Setup Time into 8284A (See Notes 1, 2)	35		35		35		ns	
TCLR1X	RDY Hold Time into 8284A (See Notes 1, 2)	0		0		0		ns	
TRYHCH	READY Setup Time into 8086	118		53		68		ns	
TCHRYX	READY Hold Time into 8086	30		20		20		ns	
TRYLCL	READY Inactive to CLK (See Note 3)	−8		−10		−8		ns	
THVCH	HOLD Setup Time	35		20		20		ns	
TINVCH	INTR, NMI, $\overline{\text{TEST}}$ Setup Time (See Note 2)	30		15		15		ns	
TILIH	Input Rise Time (Except CLK)		20		20		20	ns	From 0.8V to 2.0V
TIHIL	Input Fall Time (Except CLK)		12		12		12	ns	From 2.0V to 0.8V

A.C. CHARACTERISTICS (Continued)

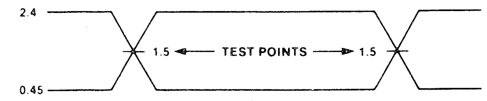
TIMING RESPONSES

Symbol	Parameter	5MHz 8086		10MHz 8086-1 (Preliminary)		8MHz 8086-2		Units	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
TCLAV	Address Valid Delay	10	110	10	50	10	60	ns	*C_L = 20-100 pF for all 8086 Outputs (In addition to 8086 self-load)
TCLAX	Address Hold Time	10		10		10		ns	
TCLAZ	Address Float Delay	TCLAX	80	10	40	TCLAX	50	ns	
TLHLL	ALE Width	TCLCH−20		TCLCH−10		TCLCH-10		ns	
TCLLH	ALE Active Delay		80		40		50	ns	
TCHLL	ALE Inactive Delay		85		45		55	ns	
TLLAX	Address Hold Time to ALE Inactive	TCHCL−10		TCHCL−10		TCHCL−10		ns	
TCLDV	Data Valid Delay	10	110	10	50	10	60	ns	
TCHDX	Data Hold Time	10		10		10		ns	
TWHDX	Data Hold Time After WR	TCLCH−30		TCLCH−25		TCLCH−30		ns	
TCVCTV	Control Active Delay 1	10	110	10	50	10	70	ns	
TCHCTV	Control Active Delay 2	10	110	10	45	10	60	ns	
TCVCTX	Control Inactive Delay	10	110	10	50	10	70	ns	
TAZRL	Address Float to READ Active	0		0		0		ns	
TCLRL	$\overline{RD}$ Active Delay	10	165	10	70	10	100	ns	
TCLRH	$\overline{RD}$ Inactive Delay	10	150	10	60	10	80	ns	
TRHAV	$\overline{RD}$ Inactive to Next Address Active	TCLCL−45		TCLCL−35		TCLCL−40		ns	
TCLHAV	HLDA Valid Delay	10	160	10	60	10	100	ns	
TRLRH	$\overline{RD}$ Width	2TCLCL−75		2TCLCL−40		2TCLCL−50		ns	
TWLWH	$\overline{WR}$ Width	2TCLCL−60		2TCLCL−35		2TCLCL−40		ns	
TAVAL	Address Valid to ALE Low	TCLCH−60		TCLCH−35		TCLCH−40		ns	
TOLOH	Output Rise Time		20		20		20	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		12		12		12	ns	From 2.0V to 0.8V

NOTES:
1. Signal at 8284A shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T2 state. (8 ns into T3).

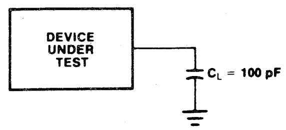
5

A.C. TESTING INPUT, OUTPUT WAVEFORM



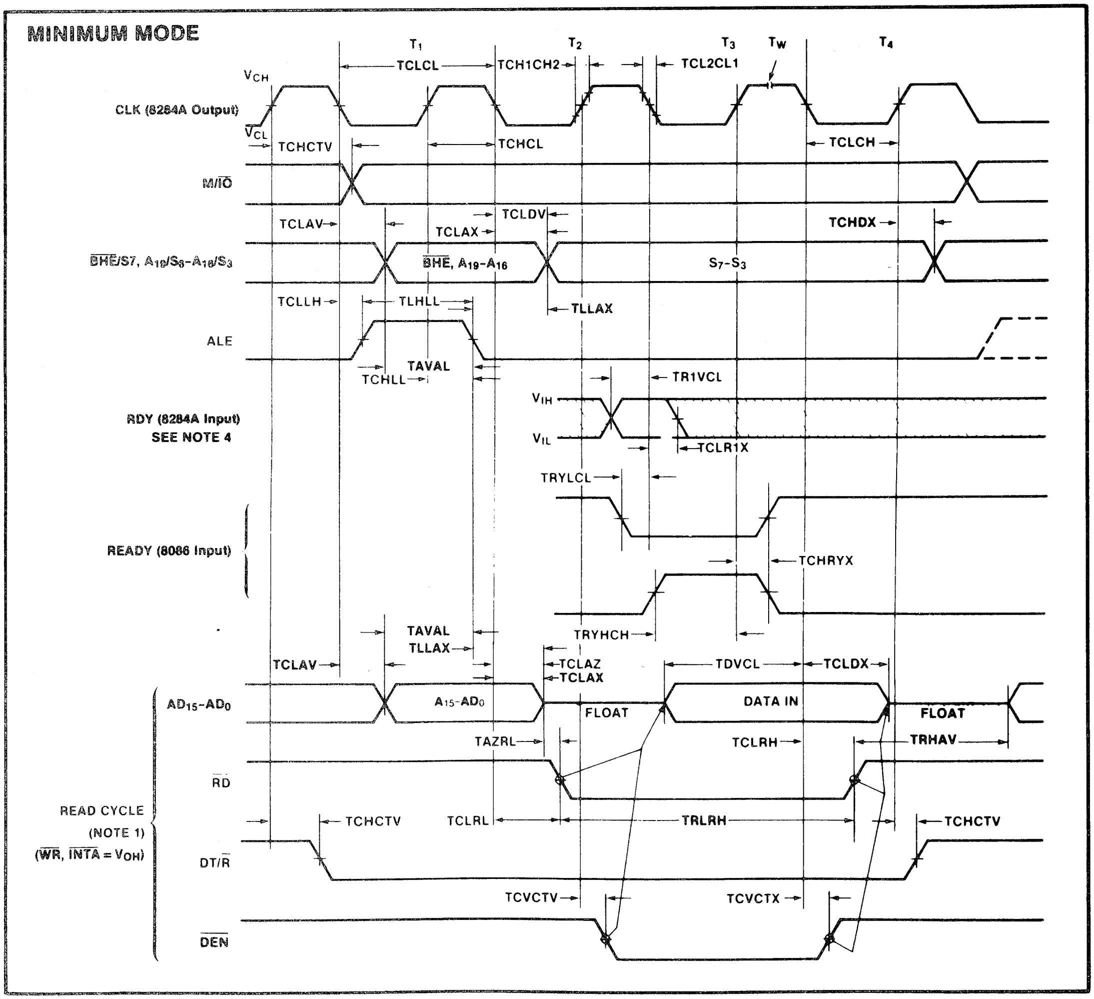
A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 1.5V FOR BOTH A LOGIC "1" AND "0".

A.C. TESTING LOAD CIRCUIT



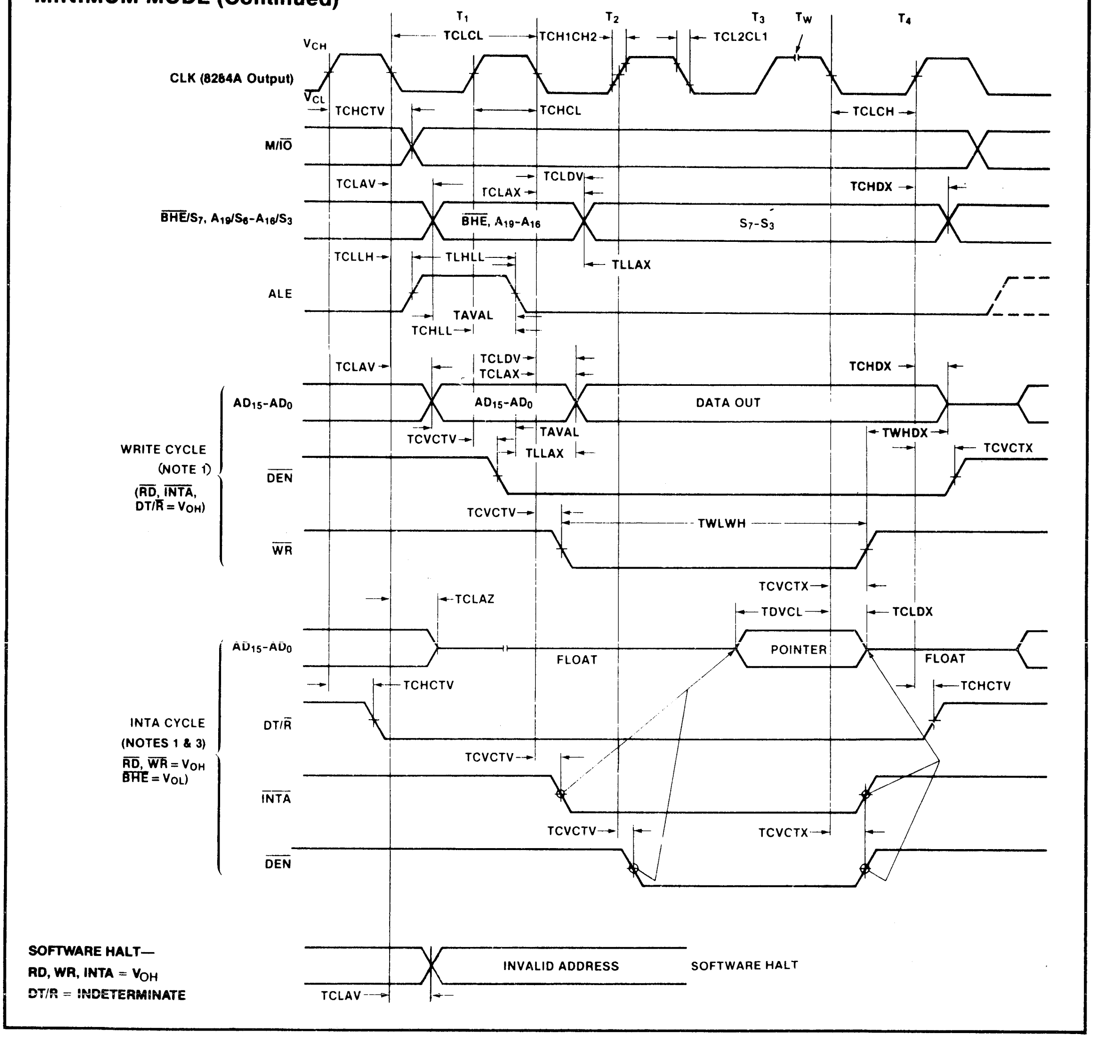
C_L INCLUDES JIG CAPACITANCE

WAVEFORMS



WAVEFORMS (Continued)

MINIMUM MODE (Continued)



NOTES:

1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. RDY is sampled near the end of T_2, T_3, T_W to determine if T_W machines states are to be inserted.
3. Two INTA cycles run back-to-back. The 8086 LOCAL ADDR/DATA BUS is floating during both INTA cycles. Control signals shown for second INTA cycle.
4. Signals at 8284A are shown for reference only.
5. All timing measurements are made at 1.5V unless otherwise noted.

5

A.C. CHARACTERISTICS

MAX MODE SYSTEM (USING 8288 BUS CONTROLLER) TIMING REQUIREMENTS

Symbol	Parameter	5MHz 8086		10MHz 8086-1 (Preliminary)		8MHz 8086-2 (Preliminary)		Units	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
TCLCL	CLK Cycle Period	200	500	100	500	125	500	ns	
TCLCH	CLK Low Time	118		53		68		ns	
TCHCL	CLK High Time	69		39		44		ns	
TCH1CH2	CLK Rise Time		10		10		10	ns	From 1.0V to 3.5V
TCL2CL1	CLK Fall Time		10		10		10	ns	From 3.5V to 1.0V
TDVCL	Data in Setup Time	30		5		20		ns	
TCLDX	Data In Hold Time	10		10		10		ns	
TR1VCL	RDY Setup Time into 8284A (See Notes 1, 2)	35		35		35		ns	
TCLR1X	RDY Hold Time into 8284A (See Notes 1, 2)	0		0		0		ns	
TRYHCH	READY Setup Time into 8086	118		53		68		ns	
TCHRYX	READY Hold Time into 8086	30		20		20		ns	
TRYLCL	READY Inactive to CLK (See Note 4)	−8		−10		−8		ns	
TINVCH	Setup Time for Recognition (INTR, NMI, $\overline{\text{TEST}}$) (See Note 2)	30		15		15		ns	
TGVCH	$\overline{\text{RQ}}/\overline{\text{GT}}$ Setup Time	30		12		15		ns	
TCHGX	$\overline{\text{RQ}}$ Hold Time into 8086	40		20		30		ns	
TILIH	Input Rise Time (Except CLK)		20		20		20	ns	From 0.8V to 2.0V
TIHIL	Input Fall Time (Except CLK)		12		12		12	ns	From 2.0V to 0.8V

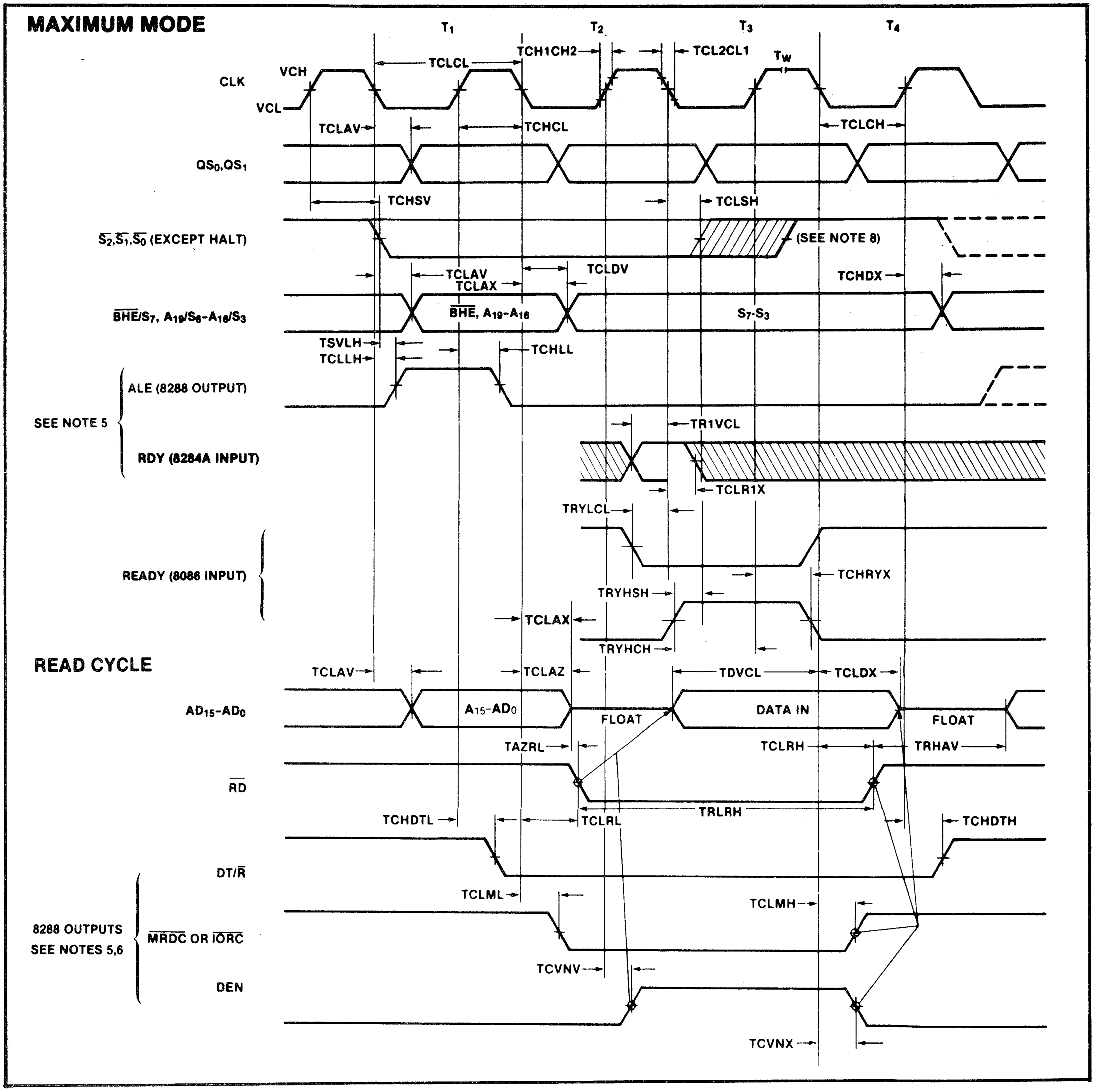
NOTES:
1. Signal at 8284A or 8288 shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T3 and wait states.
4. Applies only to T2 state (8 ns into T3).

A.C. CHARACTERISTICS (Continued)

TIMING RESPONSES

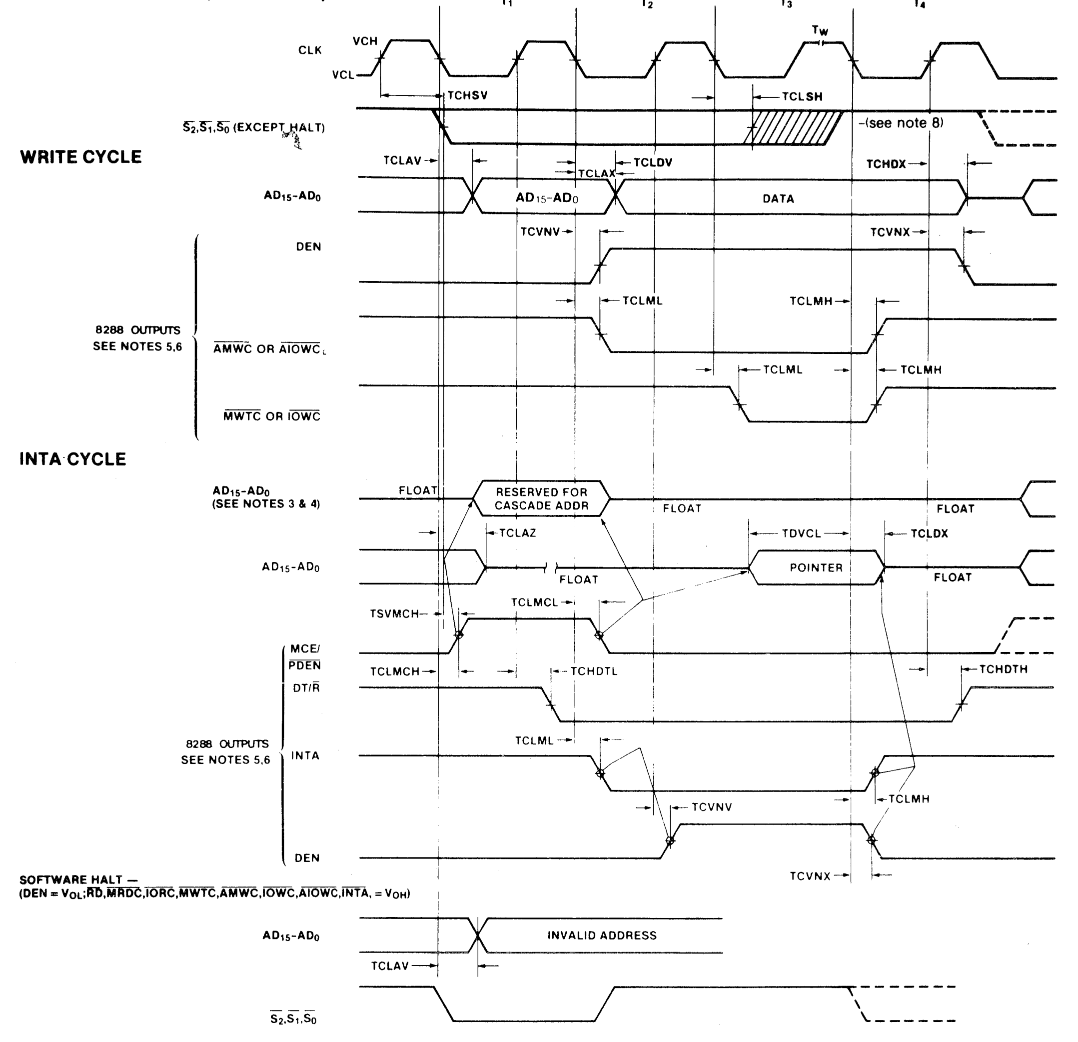
Symbol	Parameter	5MHz 8086		10MHz 8086-1 (Preliminary)		8MHz 8086-2 (Preliminary)		Units	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
TCLML	Command Active Delay (See Note 1)	10	35	10	35	10	35	ns	
TCLMH	Command Inactive Delay (See Note 1)	10	35	10	35	10	35	ns	
TRYHSH	READY Active to Status Passive (See Note 3)		110		45		65	ns	
TCHSV	Status Active Delay	10	110	10	45	10	60	ns	
TCLSH	Status Inactive Delay	10	130	10	55	10	70	ns	
TCLAV	Address Valid Delay	10	110	10	50	10	60	ns	
TCLAX	Address Hold Time	10		10		10		ns	
TCLAZ	Address Float Delay	TCLAX	80	10	40	TCLAX	50	ns	
TSVLH	Status Valid to ALE High (See Note 1)		15		15		15	ns	
TSVMCH	Status Valid to MCE High (See Note 1)		15		15		15	ns	
TCLLH	CLK Low to ALE Valid (See Note 1)		15		15		15	ns	
TCLMCH	CLK Low to MCE High (See Note 1)		15		15		15	ns	
TCHLL	ALE Inactive Delay (See Note 1)		15		15		15	ns	C_L = 20-100 pF for all 8086 Outputs (In addition to 8086 self-load)
TCLMCL	MCE Inactive Delay (See Note 1)		15		15		15	ns	
TCLDV	Data Valid Delay	10	110	10	50	10	60	ns	
TCHDX	Data Hold Time	10		10		10		ns	
TCVNV	Control Active Delay (See Note 1)	5	45	5	45	5	45	ns	
TCVNX	Control Inactive Delay (See Note 1)	10	45	10	45	10	45	ns	
TAZRL	Address Float to Read Active	0		0		0		ns	
TCLRL	RD Active Delay	10	165	10	70	10	100	ns	
TCLRH	RD Inactive Delay	10	150	10	60	10	80	ns	
TRHAV	RD Inactive to Next Address Active	TCLCL−45		TCLCL−35		TCLCL−40		ns	
TCHDTL	Direction Control Active Delay (See Note 1)		50		50		50	ns	
TCHDTH	Direction Control Inactive Delay (See Note 1)		30		30		30	ns	
TCLGL	GT Active Delay	0	85	0	45	0	50	ns	
TCLGH	GT Inactive Delay	0	85	0	45	0	50	ns	
TRLRH	RD Width	2TCLCL−75		2TCLCL−40		2TCLCL−50		ns	
TOLOH	Output Rise Time		20		20		20	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		12		12		12	ns	From 2.0V to 0.8V

WAVEFORMS


MAXIMUM MODE
T1
T2
T3
T4
TCLCL
TCH1CH2
TCL2CL1
TW
CLK
VCH
VCL
TCLAV
TCHCL
TCLCH
QS0,QS1
TCHSV
TCLSH
S2,S1,S0 (EXCEPT HALT)
(SEE NOTE 8)
TCLAV
TCLAX
TCLDV
TCHDX
BHE/S7, A19/S6-A16/S3
BHE, A19-A16
S7-S3
TSVLH
TCLLH
TCHLL
SEE NOTE 5
ALE (8288 OUTPUT)
TR1VCL
RDY (8284A INPUT)
TCLR1X
TRYLCL
READY (8086 INPUT)
TCHRYX
TRYHSH
TCLAX
TRYHCH
READ CYCLE
TCLAV
TCLAZ
TDVCL
TCLDX
AD15-AD0
A15-AD0
FLOAT
DATA IN
FLOAT
TAZRL
TCLRH
TRHAV
RD
TCHDTL
TCLRL
TRLRH
TCHDTH
DT/R
TCLML
TCLMH
8288 OUTPUTS
SEE NOTES 5,6
MRDC OR IORC
TCVNV
DEN
TCVNX

5

MAXIMUM MODE (Continued)

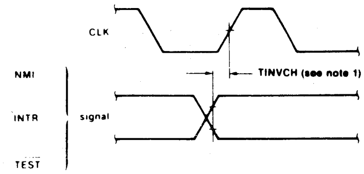


NOTES:

1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. RDY is sampled near the end of T_2, T_3, T_W to determine if T_W machines states are to be inserted.
3. Cascade address is valid between first and second INTA cycle.
4. Two INTA cycles run back-to-back. The 8086 LOCAL ADDR/DATA BUS is floating during both INTA cycles. Control for pointer address is shown for second INTA cycle.
5. Signals at 8284A or 8288 are shown for reference only.
6. The issuance of the 8288 command and control signals ($\overline{MRDC}$, $\overline{MWTC}$, $\overline{AMWC}$, $\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$ and DEN) lags the active high 8288 CEN.
7. All timing measurements are made at 1.5V unless otherwise noted.
8. Status inactive in state just prior to T_4.

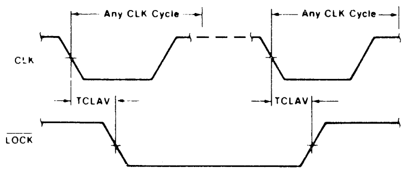
WAVEFORMS (Continued)

ASYNCHRONOUS SIGNAL RECOGNITION

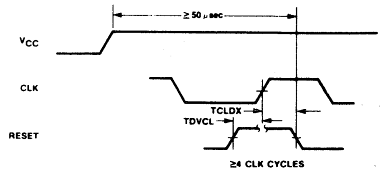


NOTE: 1 SETUP REQUIREMENTS FOR ASYNCHRONOUS SIGNALS ONLY TO GUARANTEE RECOGNITION AT NEXT CLK

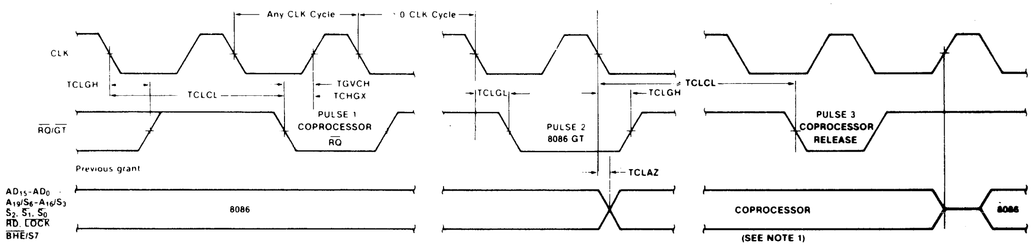
BUS LOCK SIGNAL TIMING (MAXIMUM MODE ONLY)



RESET TIMING



REQUEST/GRANT SEQUENCE TIMING (MAXIMUM MODE ONLY)



NOTES 1 THE COPROCESSOR MAY NOT DRIVE THE BUSES OUTSIDE THE REGION SHOWN WITHOUT RISKING CONTENTION

HOLD/HOLD ACKNOWLEDGE TIMING (MINIMUM MODE ONLY)

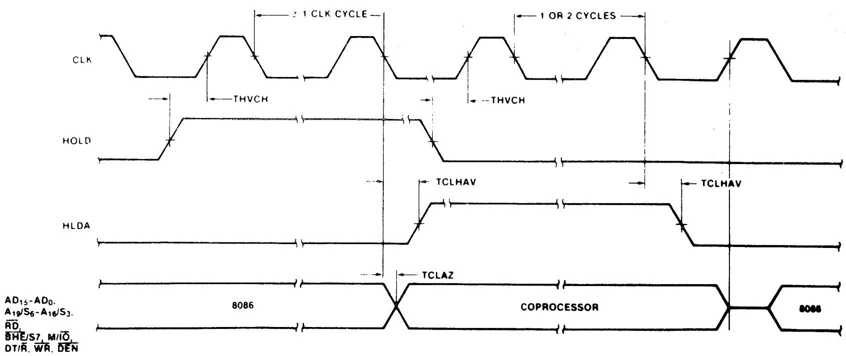


Table 2. Instruction Set Summary

DATA TRANSFER

MOV = Move:

	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Register/memory to/from register	1 0 0 0 1 0 d w	mod reg r/m		
Immediate to register/memory	1 1 0 0 0 1 1 w	mod 0 0 0 r/m	data	data if w 1
Immediate to register	1 0 1 1 w reg	data	data if w 1	
Memory to accumulator	1 0 1 0 0 0 0 w	addr low	addr-high	
Accumulator to memory	1 0 1 0 0 0 1 w	addr-low	addr-high	
Register/memory to segment register	1 0 0 0 1 1 1 0	mod 0 reg r/m		
Segment register to register/memory	1 0 0 0 1 1 0 0	mod 0 reg r/m		

PUSH = Push:

Register/memory	1 1 1 1 1 1 1 1	mod 1 1 0 r/m
Register	0 1 0 1 0 reg	
Segment register	0 0 0 reg 1 1 0	

POP = Pop:

Register/memory	1 0 0 0 1 1 1 1	mod 0 0 0 r/m
Register	0 1 0 1 1 reg	
Segment register	0 0 0 reg 1 1 1	

XCHG = Exchange:

Register/memory with register	1 0 0 0 0 1 1 w	mod reg r/m
Register with accumulator	1 0 0 1 0 reg	

IN=Input from:

Fixed port	1 1 1 0 0 1 0 w	port
Variable port	1 1 1 0 1 1 0 w	

OUT = Output to:

Fixed port	1 1 1 0 0 1 1 w	port
Variable port	1 1 1 0 1 1 1 w	
XLAT=Translate byte to AL	1 1 0 1 0 1 1 1	
LEA=Load EA to register	1 0 0 0 1 1 0 1	mod reg r/m
LDS=Load pointer to DS	1 1 0 0 0 1 0 1	mod reg r/m
LES=Load pointer to ES	1 1 0 0 0 1 0 0	mod reg r/m
LAHF=Load AH with flags	1 0 0 1 1 1 1 1	
SAHF=Store AH into flags	1 0 0 1 1 1 1 0	
PUSHF=Push flags	1 0 0 1 1 1 0 0	
POPF=Pop flags	1 0 0 1 1 1 0 1	

ARITHMETIC

ADD = Add:

Reg./memory with register to either	0 0 0 0 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 s w	mod 0 0 0 r/m	data	data if s w 01
Immediate to accumulator	0 0 0 0 0 1 0 w	data	data if w 1	

ADC = Add with carry:

Reg./memory with register to either	0 0 0 1 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 s w	mod 0 1 0 r/m	data	data if s w 01
Immediate to accumulator	0 0 0 1 0 1 0 w	data	data if w 1	

INC = Increment:

Register/memory	1 1 1 1 1 1 1 w	mod 0 0 0 r/m
Register	0 1 0 0 0 reg	
AAA=ASCII adjust for add	0 0 1 1 0 1 1 1	
DAA=Decimal adjust for add	0 0 1 0 0 1 1 1	

SUB = Subtract:

Reg./memory and register to either	0 0 1 0 1 0 d w	mod reg r/m		
Immediate from register/memory	1 0 0 0 0 0 s w	mod 1 0 1 r/m	data	data if s w 01
Immediate from accumulator	0 0 1 0 1 1 0 w	data	data if w 1	

SBB = Subtract with borrow

Reg./memory and register to either	0 0 0 1 1 0 d w	mod reg r/m		
Immediate from register/memory	1 0 0 0 0 0 s w	mod 0 1 1 r/m	data	data if s w 01
Immediate from accumulator	0 0 0 1 1 1 0 w	data	data if w 1	

DEC = Decrement:

	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Register/memory	1 1 1 1 1 1 1 w	mod 0 0 1 r/m		
Register	0 1 0 0 1 reg			
NEG Change sign	1 1 1 1 0 1 1 w	mod 0 1 1 r/m		

CMP = Compare:

Register/memory and register	0 0 1 1 1 0 d w	mod reg r/m		
Immediate with register/memory	1 0 0 0 0 0 s w	mod 1 1 1 r/m	data	data if s w 01
Immediate with accumulator	0 0 1 1 1 1 0 w	data	data if w 1	
AAS ASCII adjust for subtract	0 0 1 1 1 1 1 1			
DAS Decimal adjust for subtract	0 0 1 0 1 1 1 1			
MUL Multiply (unsigned)	1 1 1 1 0 1 1 w	mod 1 0 0 r/m		
IMUL Integer multiply (signed)	1 1 1 1 0 1 1 w	mod 1 0 1 r/m		
AAM ASCII adjust for multiply	1 1 0 1 0 1 0 0	0 0 0 0 1 0 1 0		
DIV Divide (unsigned)	1 1 1 1 0 1 1 w	mod 1 1 0 r/m		
IDIV Integer divide (signed)	1 1 1 1 0 1 1 w	mod 1 1 1 r/m		
AAD ASCII adjust for divide	1 1 0 1 0 1 0 1	0 0 0 0 1 0 1 0		
CBW Convert byte to word	1 0 0 1 1 0 0 0			
CWD Convert word to double word	1 0 0 1 1 0 0 1			

LOGIC

NOT Invert	1 1 1 1 0 1 1 w	mod 0 1 0 r/m
SHL/SAL Shift logical/arithmetic left	1 1 0 1 0 0 v w	mod 1 0 0 r/m
SHR Shift logical right	1 1 0 1 0 0 v w	mod 1 0 1 r/m
SAR Shift arithmetic right	1 1 0 1 0 0 v w	mod 1 1 1 r/m
ROL Rotate left	1 1 0 1 0 0 v w	mod 0 0 0 r/m
ROR Rotate right	1 1 0 1 0 0 v w	mod 0 0 1 r/m
RCL Rotate through carry flag left	1 1 0 1 0 0 v w	mod 0 1 0 r/m
RCR Rotate through carry right	1 1 0 1 0 0 v w	mod 0 1 1 r/m

AND = And:

Reg./memory and register to either	0 0 1 0 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 0 0 r/m	data	data if w 1
Immediate to accumulator	0 0 1 0 0 1 0 w	data	data if w 1	

TEST = And function to flags, no result:

Register/memory and register	1 0 0 0 0 1 0 w	mod reg r/m		
Immediate data and register/memory	1 1 1 1 0 1 1 w	mod 0 0 0 r/m	data	data if w 1
Immediate data and accumulator	1 0 1 0 1 0 0 w	data	data if w 1	

OR = Or:

Reg./memory and register to either	0 0 0 0 1 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 0 0 1 r/m	data	data if w 1
Immediate to accumulator	0 0 0 0 1 1 0 w	data	data if w 1	

XOR = Exclusive or:

Reg./memory and register to either	0 0 1 1 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 1 0 r/m	data	data if w 1
Immediate to accumulator	0 0 1 1 0 1 0 w	data	data if w 1	

STRING MANIPULATION

REP=Repeat	1 1 1 1 0 0 1 z
MOVS=Move byte/word	1 0 1 0 0 1 0 w
CMPS=Compare byte/word	1 0 1 0 0 1 1 w
SCAS=Scan byte/word	1 0 1 0 1 1 1 w
LODS=Load byte/wd to AL/AX	1 0 1 0 1 1 0 w
STOS=Stor byte/wd from AL/A	1 0 1 0 1 0 1 w

Table 2. Instruction Set Summary (Continued)

CONTROL TRANSFER

	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
CALL Call			
Direct within segment	1 1 1 0 1 0 0 0	disp-low	disp-high
Indirect within segment	1 1 1 1 1 1 1 1	mod 0 1 0 r m	
Direct intersegment	1 0 0 1 1 0 1 0	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	1 1 1 1 1 1 1 1	mod 0 1 1 r/m	
JMP Unconditional Jump:			
Direct within segment	1 1 1 0 1 0 0 1	disp-low	disp-high
Direct within segment short	1 1 1 0 1 0 1 1	disp	
Indirect within segment	1 1 1 1 1 1 1 1	mod 1 0 0 r m	
Direct intersegment	1 1 1 0 1 0 1 0	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	1 1 1 1 1 1 1 1	mod 1 0 1 r/m	
RET Return from CALL:			
Within segment	1 1 0 0 0 0 1 1		
Within seg adding immed to SP	1 1 0 0 0 0 1 0	data-low	data-high
Intersegment	1 1 0 0 1 0 1 1		
Intersegment adding immediate to SP	1 1 0 0 1 0 1 0	data-low	data-high
JE/JZ Jump on equal/zero	0 1 1 1 0 1 0 0	disp	
JL/JNGE Jump on less/not greater or equal	0 1 1 1 1 1 0 0	disp	
JLE/JNG Jump on less or equal/not greater	0 1 1 1 1 1 1 0	disp	
JB/JNAE Jump on below/not above or equal	0 1 1 1 0 0 1 0	disp	
JBE/JNA Jump on below or equal/not above	0 1 1 1 0 1 1 0	disp	
JP/JPE Jump on parity/parity even	0 1 1 1 1 0 1 0	disp	
JO Jump on overflow	0 1 1 1 0 0 0 0	disp	
JS Jump on sign	0 1 1 1 1 0 0 0	disp	
JNE/JNZ Jump on not equal/not zero	0 1 1 1 0 1 0 1	disp	
JNL/JGE Jump on not less/greater or equal	0 1 1 1 1 1 0 1	disp	
JNLE/JG Jump on not less or equal/greater	0 1 1 1 1 1 1 1	disp	

	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
JNB/JAE Jump on not below/above or equal	0 1 1 1 0 0 1 1	disp
JNBE/JA Jump on not below or equal/above	0 1 1 1 0 1 1 1	disp
JNP/JPO Jump on not par/par odd	0 1 1 1 1 0 1 1	disp
JNO Jump on not overflow	0 1 1 1 0 0 0 1	disp
JNS Jump on not sign	0 1 1 1 1 0 0 1	disp
LOOP Loop CX times	1 1 1 0 0 0 1 0	disp
LOOPZ/LOOPE Loop while zero/equal	1 1 1 0 0 0 0 1	disp
LOOPNZ/LOOPNE Loop while not zero/equal	1 1 1 0 0 0 0 0	disp
JCXZ Jump on CX zero	1 1 1 0 0 0 1 1	disp
INT Interrupt		
Type specified	1 1 0 0 1 1 0 1	type
Type 3	1 1 0 0 1 1 0 0	
INTO Interrupt on overflow	1 1 0 0 1 1 1 0	
IRET Interrupt return	1 1 0 0 1 1 1 1	

PROCESSOR CONTROL

CLC Clear carry	1 1 1 1 1 0 0 0	
CMC Complement carry	1 1 1 1 0 1 0 1	
STC Set carry	1 1 1 1 1 0 0 1	
CLD Clear direction	1 1 1 1 1 1 0 0	
STD Set direction	1 1 1 1 1 1 0 1	
CLI Clear interrupt	1 1 1 1 1 0 1 0	
STI Set interrupt	1 1 1 1 1 0 1 1	
HLT Halt	1 1 1 1 0 1 0 0	
WAIT Wait	1 0 0 1 1 0 1 1	
ESC Escape (to external device)	1 1 0 1 1 x x x	mod x x x r/m
LOCK Bus lock prefix	1 1 1 1 0 0 0 0	

Footnotes:

AL = 8-bit accumulator
AX = 16-bit accumulator
CX = Count register
DS = Data segment
ES = Extra segment
Above/below refers to unsigned value.
Greater = more positive;
Less = less positive (more negative) signed values
if d = 1 then "to" reg; if d = 0 then "from" reg
if w = 1 then word instruction; if w = 0 then byte instruction

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low

if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP
DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low

Mnemonics © Intel, 1978

if s:w = 01 then 16 bits of immediate data form the operand.
if s:w = 11 then an immediate data byte is sign extended to form the 16-bit operand.
if v = 0 then "count" = 1; if v = 1 then "count" in (CL)
x = don't care
z is used for string primitives for comparison with Z.F FLAG.

SEGMENT OVERRIDE PREFIX

0 0 1 reg 1 1 0

REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)	Segment
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	
101 BP	101 CH	
110 SI	110 DH	
111 DI	111 BH	

Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:

FLAGS = X:X:X:X:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

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ORDERING INFORMATION

Part number	Temperature range	Freq. (MHz)	Vcc (V)	Package
D-8086	Commercial 0 - 70° C	5	5 V ± 10 %	Cerdip
D-8086-2	0 - 70° C	8	5 V ± 5 %	Cerdip
D-8086-1	0 - 70° C	10	5 V ± 5 %	Cerdip

MHS
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M 8086
16-BIS HMOS MICROPROCESSOR

MILITARY

- **Full Military Temperature Range: -55° C to +125° C**
- **Direct Addressing Capability to 1 MByte of Memory**
- **Assembly Language Compatible with 8080/8085**
- **14 Word, By 16-Bit Register Set with Symmetrical Operations**
- **24 Operand Addressing Modes**
- **Bit, Byte, Word, and Block Operations**
- **8-and 16-Bit Signed and Unsigned Arithmetic in Binary or Decimal Including Multiply and Divide**
- **5 MHz Clock Rate**
- **MULTIBUS™ System Compatible Interface**

The MHS 8086 is a new generation, high performance microprocessor implemented in N-channel, depletion load, silicon gate technology (HMOS), and packaged in a 40-pin CerDIP package. The processor has attributes of both 8- and 16-bit microprocessors. It addresses memory as a sequence of 8-bit bytes, but has a 16-bit wide physical path to memory for high performance.

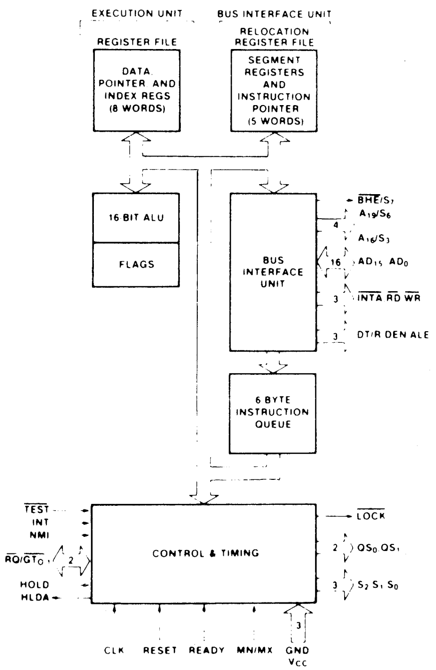

Figure 1. M 8086 **Functional Block Diagram**

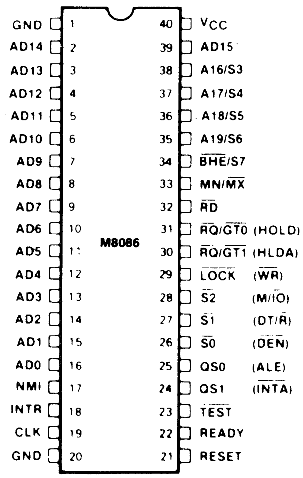

Figure 2. M 8086 **Pin Configuration**

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias .... −55°C to +125°C
Storage Temperature .... −65°C to +150°C
Voltage on Any Pin with
Respect to Ground .... −1.0 to +7V
Power Dissipation .... 2.5 Watt

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

MD-8086 (cerdip)(5 mHZ)
D.C. CHARACTERISTICS (T_A = −55°C to +125°C, V_{CC} = 5V ±10%)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	−0.5	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
I_{CC}	Power Supply Current		340	mA	T_A = 25°C
I_{LI}	Input Leakage Current		±10	μA	0V < V_{IN} < V_{CC}
I_{LO}	Output Leakage Current		±10	μA	0.45V ≤ V_{OUT} ≤ V_{CC}
V_{CL}	Clock Input Low Voltage	−0.5	+0.6	V	
V_{CH}	Clock Input High Voltage	3.9	V_{CC} + 1.0	V	
C_{IN}	Capacitance of Input Buffer (All input except $AD_0 - AD_{15}$, $\overline{RQ}/\overline{GT}$)		15	pF	fc = 1 MHz
C_{IO}	Capacitance of I/O Buffer ($AD_0 - AD_{15}$, $\overline{RQ}/\overline{GT}$)		15	pF	fc = 1 MHz

MD-8086

A.C. CHARACTERISTICS (T_A = −55°C to +125°C, V_{CC} = 5V ±10%)

MINIMUM COMPLEXITY SYSTEM TIMING REQUIREMENTS

Symbol	Parameter	8086 (5 mHZ) Min	8086 (5 mHZ) Max	Units	Test Conditions
TCLCL	CLK Cycle Period — 8086	200	500	ns	
TCLCH	CLK Low Time	(2/3 TCLCL)-15		ns	
TCHCL	CLK High Time	(1/3 TCLCL)+2		ns	
TCH1CH2	CLK Rise Time		10	ns	From 1.0V to 35.V
TCL2CL1	CLK Fall Time		10	ns	From 3.5V to 1.0V
TDVCL	Data in Setup Time	30		ns	
TCLDX	Data In Hold Time	10		ns	
TR1VCL	RDY Setup Time into 8284 (See Notes 1, 2)	35		ns	
TCLR1X	RDY Hold Time into 8284 (See Notes, 1, 2)	0		ns	
TRYHCH	READY Setup Time Into 8086	(2/3 TCLCL)-15		ns	
TCHRYX	READY Hold Time Into 8086	30		ns	
TRYLCL	READY Inactive to CLK (See Note 3)	-8		ns	
THVCH	HOLD Setup Time	35		ns	
TINVCH	INTR, NMI, $\overline{\text{TEST}}$ Setup Time (See Note 2)	30		ns	

TIMING RESPONSES

Symbol	Parameter	8086 5 mHZ Min	8086 5 mHZ Max	Units	Test Conditions
TCLAV	Address Valid Delay	10	110	ns	C_L = 20-100 pF for all 8086 Outputs (In addition to 8086 self-load)
TCLAX	Address Hold Time	10		ns	
TCLAZ	Address Float Delay	TCLAX	80	ns	
TLHLL	ALE Width	TCLCH-20		ns	
TCLLH	ALE Active Delay		80	ns	
TCHLL	ALE Inactive Delay		85	ns	
TLLAX	Address Hold Time to ALE Inactive	TCHCL-10		ns	
TCLDV	Data Valid Delay	10	110	ns	
TCHDX	Data Hold Time	10		ns	
TWHDX	Data Hold Time After WR	TCLCH-30		ns	
TCVCTV	Control Active Delay 1	10	110	ns	
TCHCTV	Control Active Delay 2	10	110	ns	
TCVCTX	Control Inactive Delay	10	110	ns	
TAZRL	Address Float to READ Active	0		ns	
TCLRL	$\overline{\text{RD}}$ Active Delay	10	165	ns	
TCLRH	$\overline{\text{RD}}$ Inactive Delay	10	150	ns	
TRHAV	$\overline{\text{RD}}$ Inactive to Next Address Active	TCLCL-45		ns	
TCLHAV	HLDA Valid Delay	10	160	ns	
TRLRH	$\overline{\text{RD}}$ Width	2TCLCL-75		ns	
TWLWH	$\overline{\text{WR}}$ Width	2TCLCL-60		ns	
TAVAL	Address Valid to ALE Low	TCLCH-60		ns	

NOTES:

1. Signal at 8284 shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T2 state (8 ns into T3).

MD-8086

A.C. CHARACTERISTICS

MAX MODE SYSTEM (USING 8288 BUS CONTROLLER) TIMING REQUIREMENTS

Symbol	Parameter	8086 (5 mHZ) Min	Max	Units	Test Conditions
TCLCL	CLK Cycle Period — 8086	200	500	ns	
TCLCH	CLK Low Time	(⅔ TCLCL) − 15		ns	
TCHCL	CLK High Time	(⅓ TCLCL) + 2		ns	
TCH1CH2	CLK Rise Time		10	ns	From 1.0V to 3.5V
TCL2CL1	CLK Fall Time		10	ns	From 3.5V to 1.0V
TDVCL	Data in Setup Time	30		ns	
TCLDX	Data in Hold Time	10		ns	
TR1VCL	RDY Setup Time into 8284 (See Notes 1, 2)	35		ns	
TCLR1X	RDY Hold Time into 8284 (See Notes 1, 2)	0		ns	
TRYHCH	Ready Setup Time into 8086	(⅔ TCLCL) − 15		ns	
TCHRYX	Ready Hold Time into 8086	30		ns	
TRYLCL	READY Inactive to CLK (See Note 4)	−8		ns	
TINVCH	Setup Time for Recognition (INTR, NMI, TEST) (See Note 2)	30		ns	
TGVCH	RQ/GT Setup Time	30		ns	
TCHGX	RQ Hold Time into 8086	40		ns	
TILIH	Input Rise Time (Except CLK)		20	ns	From 0.8V to 2.0V
TIHIL	Input Fall Time (Except CLK)		12	ns	From 2.0V to 0.8V

TIMING RESPONSES

Symbol	Parameter	8086 5 mHZ Min	Max	Units	Test Conditions
TCLML	Command Active Delay (See Note 1)	10	35	ns	C_L = 20–100 pF for all 8086 Outputs (In addition to 8086 self-load)
TCLMH	Command Inactive Delay (See Note 1)	10	35	ns	
TRYHSH	READY Active to Status Passive (See Note 3)		110	ns	
TCHSV	Status Active Delay	10	110	ns	
TCLSH	Status Inactive Delay	10	130	ns	
TCLAV	Address Valid Delay	10	110	ns	
TCLAX	Address Hold Time	10		ns	
TCLAZ	Address Float Delay	TCLAX	80	ns	
TSVLH	Status Valid to ALE High (See Note 1)		15	ns	
TSVMCH	Status Valid to MCE High (See Note 1)		15	ns	
TCLLH	CLK Low to ALE Valid (See Note 1)		15	ns	
TCLMCH	CLK Low to MCE High (See Note 1)		15	ns	
TCHLL	ALE Inactive Delay (See Note 1)		15	ns	
TCLMCL	MCE Inactive Delay (See Note 1)		15	ns	
TCLDV	Data Valid Delay	10	110	ns	
TCHDX	Data Hold Time	10		ns	
TCVNV	Control Active Delay (See Note 1)	5	45	ns	
TCVNX	Control Inactive Delay (See Note 1)	10	45	ns	
TAZRL	Address Float to Read Active	0		ns	
TCLRL	RD Active Delay	10	165	ns	

MD-8086

A.C. CHARACTERISTICS (Continued)

Symbol	Parameter	8086 (5 mHZ)		Units	Test Conditions
		Min.	Max.		
TCLRH	RD Inactive Delay	10	150	ns	
TRHAV	RD Inactive to Next Address Active	TCLCL-45		ns	
TCHDTL	Direction Control Active Delay (See Note 1)		50	ns	
TCHDTH	Direction Control Inactive Delay (See Note 1)		30	ns	
TCLGL	GT Active Delay	0	85	ns	
TCLGH	GT Inactive Delay	0	85	ns	
TRLRH	RD Width	2TCLCL-75		ns	
TOLOH	Output Rise Time		20	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		12	ns	From 2.0V to 0.8V

NOTES:
1. Signal at 8284 or 8288 shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T3 and wait states.
4. Applies only to T2 state (8 ns into T3).

ORDERING INFORMATION

Part number	Temperature range	Freq. (mHZ)	Vcc (V)	Package
MD-8086	− 55° to + 125° C no burn-in	5	5 V ± 10 %	cerdip
MD-8086/B	− 55° to + 125° C MIL 883 cond. B	5	5 V ± 10 %	cerdip

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8088
8-BIT HMOS MICROPROCESSOR

PRELIMINARY

- 8-Bit Data Bus Interface
- 16-Bit Internal Architecture
- Direct Addressing Capability to 1 Mbyte of Memory
- Direct Software Compatibility with 8086
- 14-Word by 16-Bit Register Set with Symmetrical Operations
- 24 Operand Addressing Modes
- Byte, Word, and Block Operations
- 8-Bit and 16-Bit Signed and Unsigned Arithmetic in Binary or Decimal, Including Multiply and Divide
- Compatible with 8155-2, 8755A-2 and 8185-2 Multiplexed Peripherals
- Two Clock Rates:
  5 MHz for 8088
  8 MHz for 8088-2

The MHS 8088 is a new generation, high performance microprocessor implemented in N-channel, depletion load, silicon gate technology (HMOS), and packaged in a 40-pin CerDIP package. The processor has attributes of both 8- and 16-bit microprocessors. It is directly compatible with 8086 software and 8080/8085 hardware and peripherals.

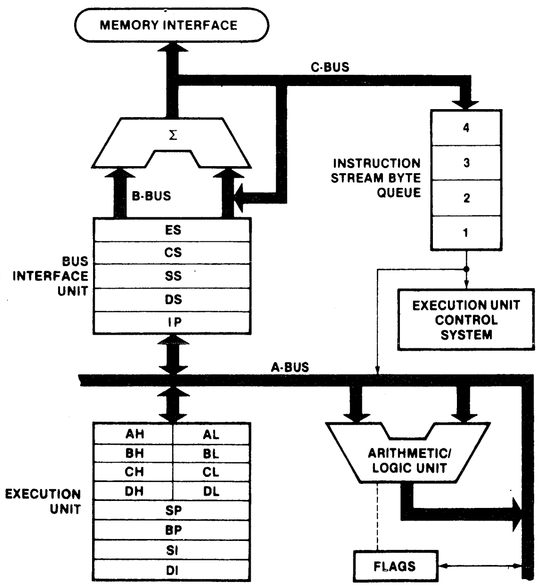

Figure 1. 8088 CPU Functional Block Diagram

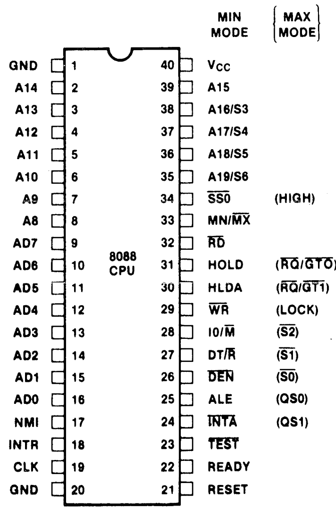

Figure 2. 8088 Pin Configuration

Table 1. Pin Description

The following pin function descriptions are for 8088 systems in either minimum or maximum mode. The "local bus" in these descriptions is the direct multiplexed bus interface connection to the 8088 (without regard to additional bus buffers).

<table>
<tr><th>Symbol</th><th>Pin No.</th><th>Type</th><th>Name and Function</th></tr>
<tr><td>AD7–AD0</td><td>9-16</td><td>I/O</td><td>Address Data Bus: These lines constitute the time multiplexed memory/IO address (T1) and data (T2, T3, Tw, and T4) bus. These lines are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge".</td></tr>
<tr><td>A15–A8</td><td>2-8, 39</td><td>O</td><td>Address Bus: These lines provide address bits 8 through 15 for the entire bus cycle (T1–T4). These lines do not have to be latched by ALE to remain valid. A15–A8 are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge".</td></tr>
<tr><td>A19/S6, A18/S5, A17/S4, A16/S3</td><td>34-38</td><td>O</td><td>Address/Status: During T1, these are the four most significant address lines for memory operations. During I/O operations, these lines are LOW. During memory and I/O operations, status information is available on these lines during T2, T3, Tw, and T4. S6 is always low. The status of the interrupt enable flag bit (S5) is updated at the beginning of each clock cycle. S4 and S3 are encoded as shown.
<table>
<tr><th>S4</th><th>S3</th><th>CHARACTERISTICS</th></tr>
<tr><td>0 (LOW)</td><td>0</td><td>Alternate Data</td></tr>
<tr><td>0</td><td>1</td><td>Stack</td></tr>
<tr><td>1 (HIGH)</td><td>0</td><td>Code or None</td></tr>
<tr><td>1</td><td>1</td><td>Data</td></tr>
<tr><td>S6 is 0 (LOW)</td><td></td><td></td></tr>
</table>
This information indicates which segment register is presently being used for data accessing.
These lines float to 3-state OFF during local bus "hold acknowledge".</td></tr>
<tr><td>$\overline{RD}$</td><td>32</td><td>O</td><td>Read: Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the IO/$\overline{M}$ pin or S2. This signal is used to read devices which reside on the 8088 local bus. $\overline{RD}$ is active LOW during T2, T3 and Tw of any read cycle, and is guaranteed to remain HIGH in T2 until the 8088 local bus has floated.
This signal floats to 3-state OFF in "hold acknowledge".</td></tr>
<tr><td>READY</td><td>22</td><td>I</td><td>READY: is the acknowledgement from the addressed memory or I/O device that it will complete the data transfer. The RDY signal from memory or I/O is synchronized by the 8284 clock generator to form READY. This signal is active HIGH. The 8088 READY input is not synchronized. Correct operation is not guaranteed if the set up and hold times are not met.</td></tr>
<tr><td>INTR</td><td>18</td><td>I</td><td>Interrupt Request: is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.</td></tr>
<tr><td>$\overline{TEST}$</td><td>23</td><td>I</td><td>$\overline{TEST}$: input is examined by the "wait for test" instruction. If the $\overline{TEST}$ input is LOW, execution continues, otherwise the processor waits in an "idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.</td></tr>
<tr><td>NMI</td><td>17</td><td>I</td><td>Non-Maskable Interrupt: is an edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from a LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.</td></tr>
</table>

Table 1. Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
RESET	21	I	**RESET:** causes the processor to immediately terminate its present activity. The signal must be active HIGH for at least four clock cycles. It restarts execution, as described in the instruction set description, when RESET returns LOW. RESET is internally synchronized.
CLK	19	I	**Clock:** provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.
V_{CC}	40		**V_{CC}:** is the +5V ±10% power supply pin.
GND	1, 20		**GND:** are the ground pins.
MN/$\overline{MX}$	33	I	**Minimum/Maximum:** indicates what mode the processor is to operate in. The two modes are discussed in the following sections.

The following pin function descriptions are for the 8088 minimum mode (i.e., MN/MX = V_{CC}). Only the pin functions which are unique to minimum mode are described; all other pin functions are as described above.

IO/$\overline{M}$	28	O	**Status Line:** is an inverted maximum mode $\overline{S2}$. It is used to distinguish a memory access from an I/O access. IO/$\overline{M}$ becomes valid in the T4 preceding a bus cycle and remains valid until the final T4 of the cycle (I/O=HIGH, M=LOW). IO/$\overline{M}$ floats to 3-state OFF in local bus "hold acknowledge".
$\overline{WR}$	29	O	**Write:** strobe indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the IO/$\overline{M}$ signal. WR is active for T2, T3, and Tw of any write cycle. It is active LOW, and floats to 3-state OFF in local bus "hold acknowledge".
$\overline{INTA}$	24	O	**INTA:** is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T2, T3, and Tw of each interrupt acknowledge cycle.
ALE	25	O	**Address Latch Enable:** is provided by the processor to latch the address into the 8282/8283 address latch. It is a HIGH pulse active during clock low of T1 of any bus cycle. Note that ALE is never floated.
DT/$\overline{R}$	27	O	**Data Transmit/Receive:** is needed in a minimum system that desires to use an 8286/8287 data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically, DT/$\overline{R}$ is equivalent to $\overline{S1}$ in the maximum mode, and its timing is the same as for IO/$\overline{M}$ (T=HIGH, R=LOW). This signal floats to 3-state OFF in local "hold acknowledge".
$\overline{DEN}$	26	O	**Data Enable:** is provided as an output enable for the 8286/8287 in a minimum system which uses the transceiver. $\overline{DEN}$ is active LOW during each memory and I/O access, and for $\overline{INTA}$ cycles. For a read or $\overline{INTA}$ cycle, it is active from the middle of T2 until the middle of T4, while for a write cycle, it is active from the beginning of T2 until the middle of T4. $\overline{DEN}$ floats to 3-state OFF during local bus "hold acknowledge".
HOLD, HLDA	30,31	I, O	**HOLD:** indicates that another master is requesting a local bus "hold". To be acknowledged, HOLD must be active HIGH. The processor receiving the "hold" request will issue HLDA (HIGH) as an acknowledgement, in the middle of a T4 or TI clock cycle. Simultaneous with the issuance of HLDA the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor lowers HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. Hold is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the set up time.
$\overline{SSO}$	34	O	**Status line:** is logically equivalent to $\overline{SO}$ in the maximum mode. The combination of SSO, IO/$\overline{M}$ and DT/$\overline{R}$ allows the system to completely decode the current bus cycle status.

IO/$\overline{M}$	DT/$\overline{R}$	$\overline{SSO}$	CHARACTERISTICS
1 (HIGH)	0	0	Interrupt Acknowledge
1	0	1	Read I/O port
1	1	0	Write I/O port
1	1	1	Halt ·
0 (LOW)	0	0	Code access
0	0	1	Read memory
0	1	0	Write memory
0	1	1	Passive

Table 1. Pin Description (Continued)

The following pin function descriptions are for the 8088, 8228 system in maximum mode (i.e., MN/MX = GND.) Only the pin functions which are unique to maximum mode are described; all other pin functions are as described above.

<table>
<tr><th>Symbol</th><th>Pin No.</th><th>Type</th><th>Name and Function</th></tr>
<tr><td>$\overline{S2}$, $\overline{S1}$, $\overline{S0}$</td><td>26-28</td><td>O</td><td>
Status: is active during clock high of T4, T1, and T2, and is returned to the passive state (1,1,1) during T3 or during Tw when READY is HIGH. This status is used by the 8288 bus controller to generate all memory and I/O access control signals. Any change by $\overline{S2}$, $\overline{S1}$, or $\overline{S0}$ during T4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T3 or Tw is used to indicate the end of a bus cycle.
<table>
<tr><th>$\overline{S2}$</th><th>$\overline{S1}$</th><th>$\overline{S0}$</th><th>CHARACTERISTICS</th></tr>
<tr><td>0 (LOW)</td><td>0</td><td>0</td><td>Interrupt Acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read I/O port</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write I/O port</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Halt</td></tr>
<tr><td>1 (HIGH)</td><td>0</td><td>0</td><td>Code access</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read memory</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write memory</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Passive</td></tr>
</table>
These signals float to 3-state OFF during "hold acknowledge". During the first clock cycle after RESET becomes active, these signals are active HIGH. After this first clock, they float to 3-state OFF.
</td></tr>
<tr><td>$\overline{RQ}/\overline{GT0}$,
$\overline{RQ}/\overline{GT1}$</td><td>30, 31</td><td>I/O</td><td>
Request/Grant: pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bidirectional with $\overline{RQ}/\overline{GT0}$ having higher priority than $\overline{RQ}/\overline{GT1}$. $\overline{RQ}/\overline{GT}$ has an internal pull-up resistor, so may be left unconnected. The request/grant sequence is as follows (See Figure 8):
1. A pulse of one CLK wide from another local bus master indicates a local bus request ("hold") to the 8088 (pulse 1).
2. During a T4 or TI clock cycle, a pulse one clock wide from the 8088 to the requesting master (pulse 2), indicates that the 8088 has allowed the local bus to float and that it will enter the "hold acknowledge" state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "hold acknowledge". The same rules as for HOLD/HOLDA apply as for when the bus is released.
3. A pulse one CLK wide from the requesting master indicates to the 8088 (pulse 3) that the "hold" request is about to end and that the 8088 can reclaim the local bus at the next CLK. The CPU then enters T4.
Each master-master exchange of the local bus is a sequence of three pulses. There must be one idle CLK cycle after each bus exchange. Pulses are active LOW.
If the request is made while the CPU is performing a memory cycle, it will release the local bus during T4 of the cycle when all the following conditions are met:
1. Request occurs on or before T2.
2. Current cycle is not the low bit of a word.
3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence.
4. A locked instruction is not currently executing.
If the local bus is idle when the request is made the two possible events will follow:
1. Local bus will be released during the next clock.
2. A memory cycle will start within 3 clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied.
</td></tr>
</table>

5

Table 1. Pin Description (Continued)

<table>
<tr><th>Symbol</th><th>Pin No.</th><th>Type</th><th>Name and Function</th></tr>
<tr><td>$\overline{LOCK}$</td><td>29</td><td>O</td><td>$\overline{LOCK}$: indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active (LOW). The $\overline{LOCK}$ signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and floats to 3-state off in "hold acknowledge".</td></tr>
<tr><td>QS1, QS0</td><td>24, 25</td><td>O</td><td>Queue Status: provide status to allow external tracking of the internal 8088 instruction queue.
The queue status is valid during the CLK cycle after which the queue operation is performed.
<table><tr><th>QS1</th><th>QS0</th><th>CHARACTERISTICS</th></tr><tr><td>0 (LOW)</td><td>0</td><td>No operation</td></tr><tr><td>0</td><td>1</td><td>First byte of opcode from queue</td></tr><tr><td>1 (HIGH)</td><td>0</td><td>Empty the queue</td></tr><tr><td>1</td><td>1</td><td>Subsequent byte from queue</td></tr></table></td></tr>
<tr><td>—</td><td>34</td><td>O</td><td>Pin 34 is always high in the maximum mode.</td></tr>
</table>

5

FUNCTIONAL DESCRIPTION

Memory Organization

The processor provides a 20-bit address to memory which locates the byte being referenced. The memory is organized as a linear array of up to 1 million bytes, addressed as 00000(H) to FFFFF(H). The memory is logically divided into code, data, extra data, and stack segments of up to 64K bytes each, with each segment falling on 16-byte boundaries. (See Figure 3.)

All memory references are made relative to base addresses contained in high speed segment registers. The segment types were chosen based on the addressing needs of programs. The segment register to be selected is automatically chosen according to the rules of the following table. All information in one segment type share the same logical attributes (e.g. code or data). By structuring memory into relocatable areas of similar characteristics and by automatically selecting segment registers, programs are shorter, faster, and more structured.

Word (16-bit) operands can be located on even or odd address boundaries. For address and data operands, the least significant byte of the word is stored in the lower valued address location and the most significant byte in the next higher address location. The BIU will automatically execute two fetch or write cycles for 16-bit operands.

Certain locations in memory are reserved for specific CPU operations. (See Figure 4.) Locations from addresses FFFF0H through FFFFFH are reserved for operations including a jump to the initial system initialization routine. Following RESET, the CPU will always begin execution at location FFFF0H where the jump must be located. Locations 00000H through 003FFH are reserved for interrupt operations. Four-byte pointers consisting of a 16-bit segment address and a 16-bit offset address direct program flow to one of the 256 possible interrupt service routines. The pointer elements are assumed to have been stored at their respective places in reserved memory prior to the occurrence of interrupts.

Minimum and Maximum Modes

The requirements for supporting minimum and maximum 8088 systems are sufficiently different that they cannot be done efficiently with 40 uniquely defined pins. Consequently, the 8088 is equipped with a strap pin ($MN/\overline{MX}$) which defines the system configuration. The definition of a certain subset of the pins changes, dependent on the condition of the strap pin. When the $MN/\overline{MX}$ pin is strapped to GND, the 8088 defines pins 24 through 31 and 34 in maximum mode. When the $MN/\overline{MX}$ pin is strapped to V_{CC}, the 8088 generates bus control signals itself on pins 24 through 31 and 34.

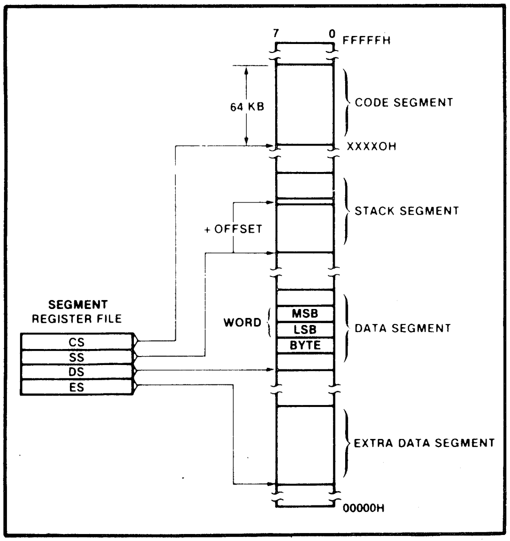

Figure 3. Memory Organization

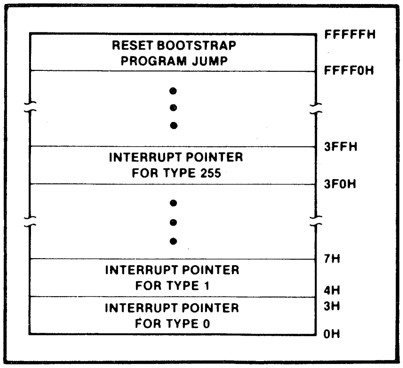

Figure 4. Reserved Memory Locations

Memory Reference Need	Segment Register Used	Segment Selection Rule
Instructions	CODE (CS)	Automatic with all instruction prefetch.
Stack	STACK (SS)	All stack pushes and pops. Memory references relative to BP base register except data references.
Local Data	DATA (DS)	Data references when: relative to stack, destination of string operation, or explicitly overridden.
External (Global) Data	EXTRA (ES)	Destination of string operations: Explicitly selected using a segment override.

The minimum mode 8088 can be used with either a multiplexed or demultiplexed bus. The multiplexed bus configuration is compatible with the MCS-85™ multiplexed bus peripherals (8155, 8156, 8355, 8755A, and 8185). This configuration (See Figure 5) provides the user with a minimum chip count system. This architecture provides the 8088 processing power in a highly integrated form.

The demultiplexed mode requires one latch (for 64K addressability) or two latches (for a full megabyte of addressing). A third latch can be used for buffering if the address bus loading requires it. An 8286 or 8287 transceiver can also be used if data bus buffering is required. (See Figure 6.) The 8088 provides $\overline{DEN}$ and DT/$\overline{R}$ to control the transceiver, and ALE to latch the addresses. This configuration of the minimum mode provides the standard demultiplexed bus structure with heavy bus buffering and relaxed bus timing requirements.

The maximum mode employs the 8288 bus controller. (See Figure 7.) The 8288 decodes status lines $\overline{S0}$, $\overline{S1}$, and $\overline{S2}$, and provides the system with all bus control signals. Moving the bus control to the 8288 provides better source and sink current capability to the control lines, and frees the 8088 pins for extended large system features. Hardware lock, queue status, and two request/grant interfaces are provided by the 8088 in maximum mode. These features allow co-processors in local bus and remote bus configurations.

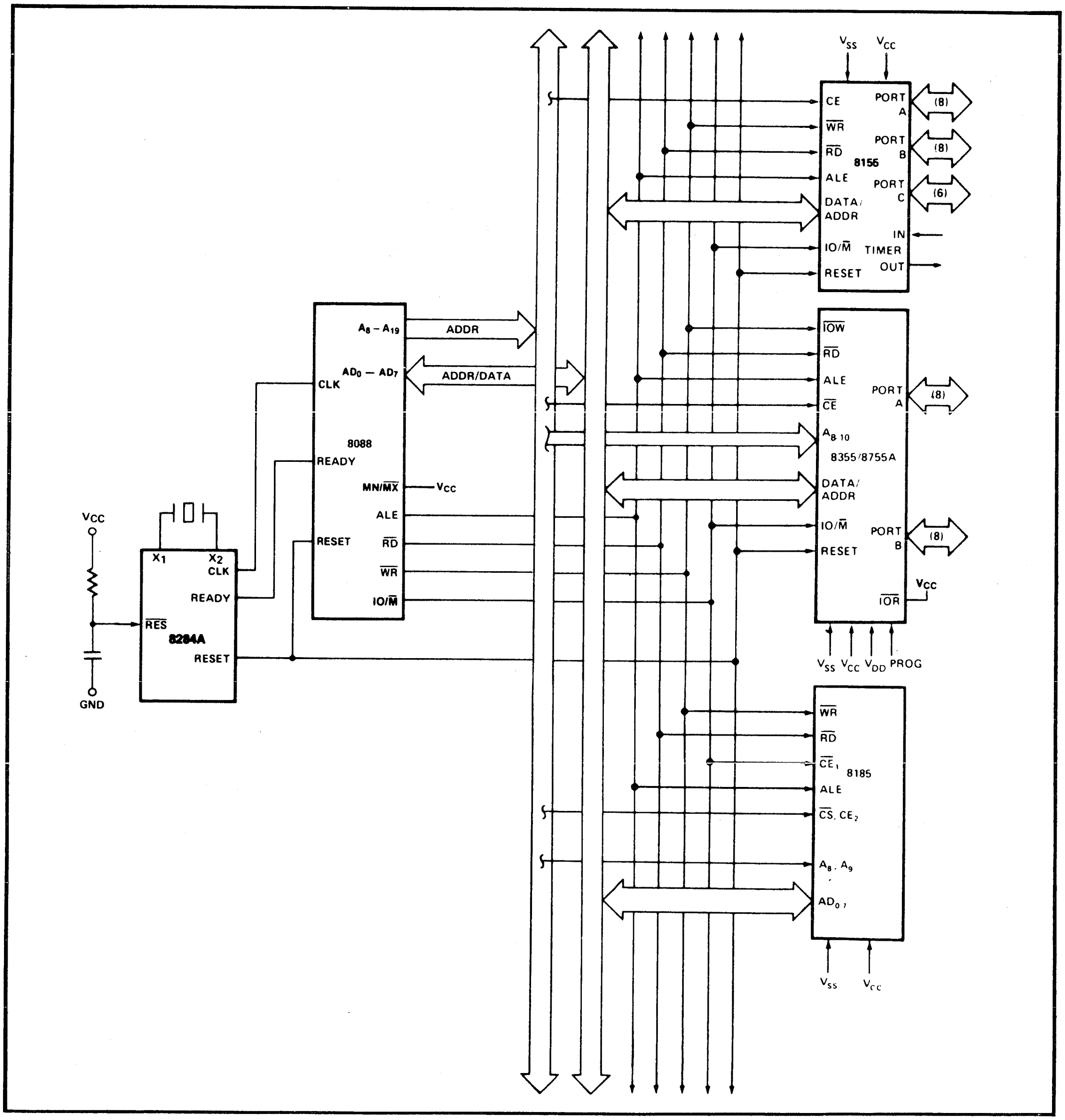

Figure 5. Multiplexed Bus Configuration

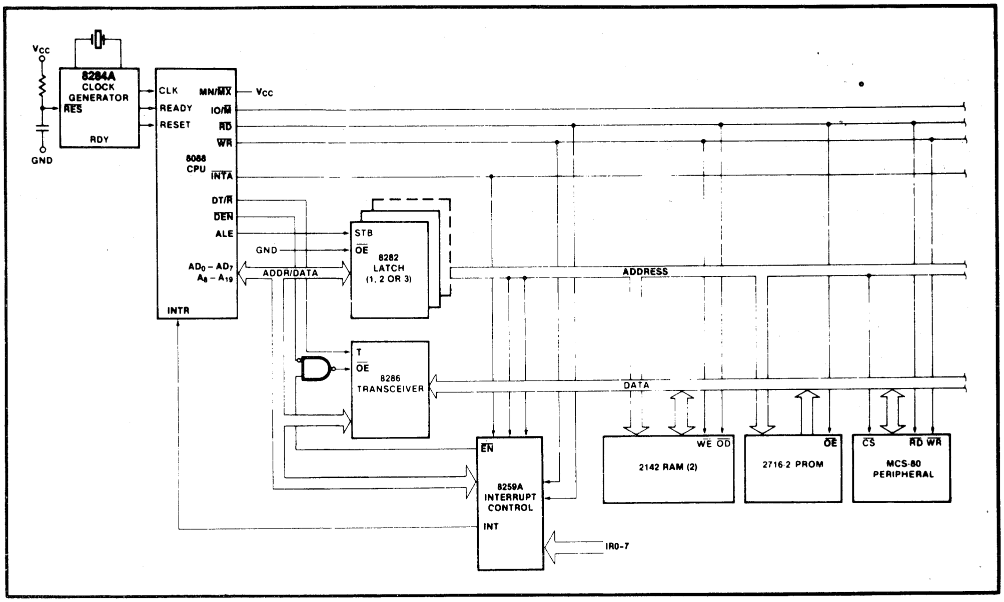

Figure 6. Demultiplexed Bus Configuration

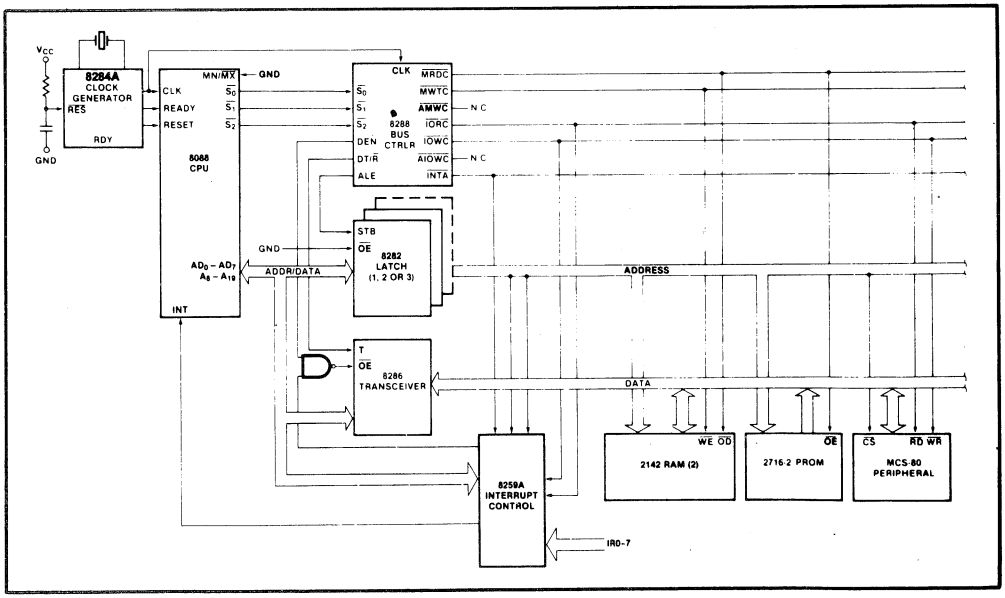

Figure 7. Fully Buffered System Using Bus Controller

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Bus Operation

The 8088 address/data bus is broken into three parts — the lower eight address/data bits (AD0–AD7), the middle eight address bits (A8–A15), and the upper four address bits (A16–A19). The address/data bits and the highest four address bits are time multiplexed. This technique provides the most efficient use of pins on the processor, permitting the use of a standard 40 lead package. The middle eight address bits are not multiplexed, i.e. they remain valid throughout each bus cycle. In addition, the bus can be demultiplexed at the processor with a single address latch if a standard, non-multiplexed bus is desired for the system.

Each processor bus cycle consists of at least four CLK cycles. These are referred to as T1, T2, T3, and T4. (See Figure 8). The address is emitted from the processor during T1 and data transfer occurs on the bus during T3 and T4. T2 is used primarily for changing the direction of the bus during read operations. In the event that a "NOT READY" indication is given by the addressed device.

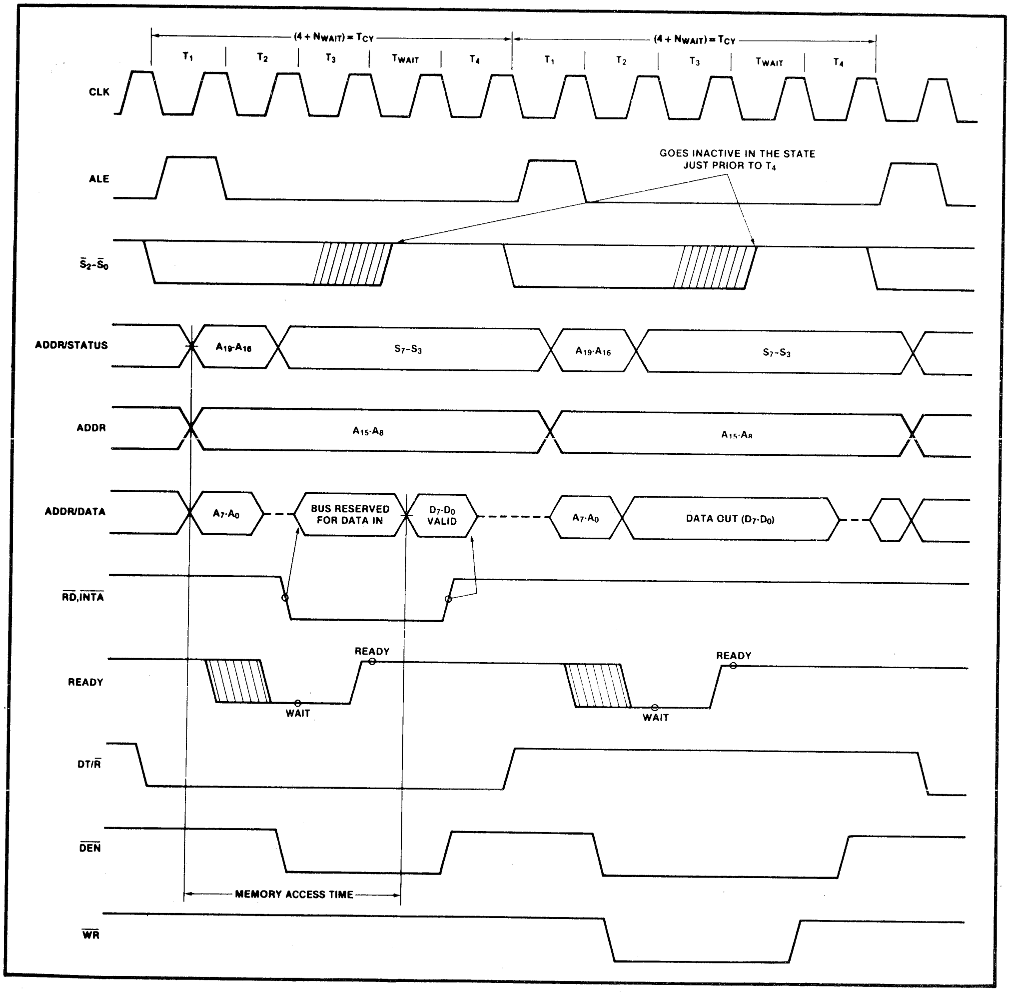


Figure 8. Basic System Timing

Bus Operation (Continued)

"wait" states (Tw) are inserted between T3 and T4. Each inserted "wait" state is of the same duration as a CLK cycle. Periods can occur between 8088 driven bus cycles. These are referred to as "idle" states (Ti), or inactive CLK cycles. The processor uses these cycles for internal housekeeping.

During T1 of any bus cycle, the ALE (address latch enable) signal is emitted (by either the processor or the 8288 bus controller, depending on the MN/$\overline{MX}$ strap). At the trailing edge of this pulse, a valid address and certain status information for the cycle may be latched.

Status bits $\overline{S0}$, $\overline{S1}$, and $\overline{S2}$ are used by the bus controller, in maximum mode, to identify the type of bus transaction according to the following table:

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	CHARACTERISTICS
0 (LOW)	0	0	Interrupt Acknowledge
0	0	1	Read I/O
0	1	0	Write I/O.
0	1	1	Halt
1 (HIGH)	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

Status bits S3 through S6 are multiplexed with high order address bits and are therefore valid during T2 through T4. S3 and S4 indicate which segment register was used for this bus cycle in forming the address according to the following table:

S_4	S_3	CHARACTERISTICS
0 (LOW)	0	Alternate Data (extra segment)
0	1	Stack
1 (HIGH)	0	Code or None
1	1	Data

S5 is a reflection of the PSW interrupt enable bit. S6 is always equal to 0.

I/O Addressing

In the 8088, I/O operations can address up to a maximum of 64K I/O registers. The I/O address appears in the same format as the memory address on bus lines A15-A0. The address lines A19-A16 are zero in I/O operations. The variable I/O instructions, which use register DX as a pointer, have full address capability, while the direct I/O instructions directly address one or two of the 256 I/O byte locations in page 0 of the I/O address space. I/O ports are addressed in the same manner as memory locations.

Designers familiar with the 8085 or upgrading an 8085 design should note that the 8085 addresses I/O with an 8-bit address on both halves of the 16-bit address bus. The 8088 uses a full 16-bit address on its lower 16 address lines.

EXTERNAL INTERFACE

Processor Reset and Initialization

Processor initialization or start up is accomplished with activation (HIGH) of the RESET pin. The 8088 RESET is required to be HIGH for greater than four clock cycles. The 8088 will terminate operations on the high-going edge of RESET and will remain dormant as long as RESET is HIGH. The low-going transition of RESET triggers an internal reset sequence for approximately 7 clock cycles. After this interval the 8088 operates normally, beginning with the instruction in absolute location FFFF0H. (See Figure 4.) The RESET input is internally synchronized to the processor clock. At initialization, the HIGH to LOW transition of RESET must occur no sooner than 50 μs after power up, to allow complete initialization of the 8088.

If INTR is asserted sooner than nine clock cycles after the end of RESET, the processor may execute one instruction before responding to the interrupt.

All 3-state outputs float to 3-state OFF during RESET. Status is active in the idle state for the first clock after RESET becomes active and then floats to 3-state OFF.

Interrupt Operations

Interrupt operations fall into two classes: software or hardware initiated. The software initiated interrupts and software aspects of hardware interrupts are specified in the instruction set description in the iAPX 88 Book or the iAPX 86, 88 User's Manual. Hardware interrupts can be classified as nonmaskable or maskable.

Interrupts result in a transfer of control to a new program location. A 256 element table containing address pointers to the interrupt service program locations resides in absolute locations 0 through 3FFH (see Figure 4), which are reserved for this purpose. Each element in the table is 4 bytes in size and corresponds to an interrupt "type." An interrupting device supplies an 8-bit type number, during the interrupt acknowledge sequence, which is used to vector through the appropriate element to the new interrupt service program location.

Non-Maskable Interrupt (NMI)

The processor provides a single non-maskable interrupt (NMI) pin which has higher priority than the maskable interrupt request (INTR) pin. A typical use would be to activate a power failure routine. The NMI is edge-triggered on a LOW to HIGH transition. The activation of this pin causes a type 2 interrupt.

NMI is required to have a duration in the HIGH state of greater than two clock cycles, but is not required to be synchronized to the clock. Any higher going transition of NMI is latched on-chip and will be serviced at the end of the current instruction or between whole moves (2 bytes in the case of word moves) of a block type instruction. Worst case response to NMI would be for multiply, divide, and variable shift instructions. There is no specification on the occurrence of the low-going edge; it may occur before, during, or after the servicing of NMI. Another high-going edge triggers another response if it occurs after the start of the NMI procedure. The signal must be free of logical spikes in general and be free of bounces on the low-going edge to avoid triggering extraneous responses.

Maskable Interrupt (INTR)

The 8088 provides a single interrupt request input (INTR) which can be masked internally by software with the resetting of the interrupt enable (IF) flag bit. The interrupt request signal is level triggered. It is internally synchronized during each clock cycle on the high-going edge of CLK. To be responded to, INTR must be present (HIGH) during the clock period preceding the end of the current instruction or the end of a whole move for a block type instruction. During interrupt response sequence, further interrupts are disabled. The enable bit is reset as part of the response to any interrupt (INTR, NMI, software interrupt, or single step), although the FLAGS register which is automatically pushed onto the stack reflects the state of the processor prior to the interrupt. Until the old FLAGS register is restored, the enable bit will be zero unless specifically set by an instruction.

During the response sequence (See Figure 9), the processor executes two successive (back to back) interrupt acknowledge cycles. The 8088 emits the LOCK signal (maximum mode only) from T2 of the first bus cycle until T2 of the second. A local bus "hold" request will not be honored until the end of the second bus cycle. In the second bus cycle, a byte is fetched from the external interrupt system (e.g., 8259A PIC) which identifies the source (type) of the interrupt. This byte is multiplied by four and used as a pointer into the interrupt vector lookup table. An INTR signal left HIGH will be continually responded to within the limitations of the enable bit and sample period. The interrupt return instruction includes a flags pop which returns the status of the original interrupt enable bit when it restores the flags.

HALT

When a software HALT instruction is executed, the processor indicates that it is entering the HALT state in one of two ways, depending upon which mode is strapped. In minimum mode, the processor issues ALE, delayed by one clock cycle, to allow the system to latch the halt status. Halt status is available on IO/$\overline{\text{M}}$, DT/$\overline{\text{R}}$, and $\overline{\text{SSO}}$. In maximum mode, the processor issues appropriate HALT status on $\overline{\text{S2}}$, $\overline{\text{S1}}$, and $\overline{\text{S0}}$, and the 8288 bus controller issues one ALE. The 8088 will not leave the HALT state when a local bus hold is entered while in HALT. In this case, the processor reissues the HALT indicator at the end of the local bus hold. An interrupt request or RESET will force the 8088 out of the HALT state.

Read/Modify/Write (Semaphore) Operations via LOCK

The LOCK status information is provided by the processor when consecutive bus cycles are required during the execution of an instruction. This allows the processor to perform read/modify/write operations on memory (via the "exchange register with memory" instruction), without another system bus master receiving intervening memory cycles. This is useful in multiprocessor system configurations to accomplish "test and set lock" operations. The $\overline{\text{LOCK}}$ signal is activated (LOW) in the clock cycle following decoding of the LOCK prefix instruction. It is deactivated at the end of the last bus cycle of the instruction following the LOCK prefix. While $\overline{\text{LOCK}}$ is active, a request on a $\overline{\text{RQ}}/\overline{\text{GT}}$ pin will be recorded, and then honored at the end of the LOCK.

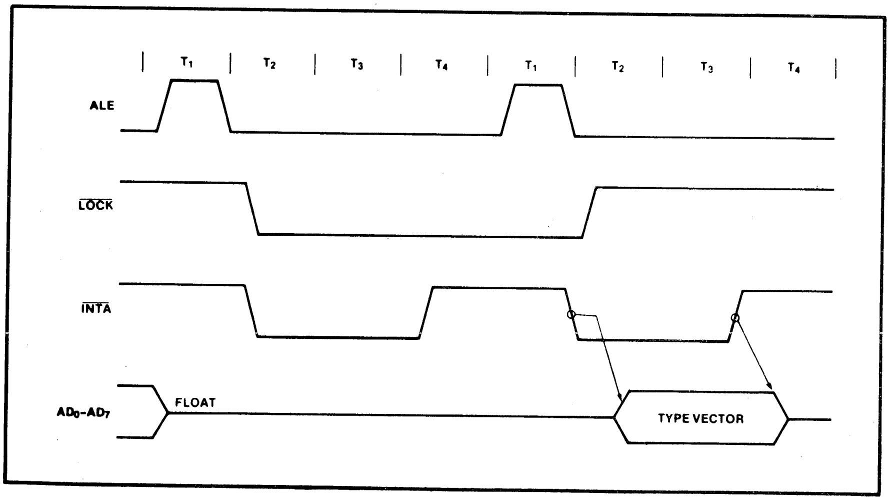


Figure 9. Interrupt Acknowledge Sequence

External Synchronization via $\overline{TEST}$

As an alternative to interrupts, the 8088 provides a single software-testable input pin ($\overline{TEST}$). This input is utilized by executing a WAIT instruction. The single WAIT instruction is repeatedly executed until the $\overline{TEST}$ input goes active (LOW). The execution of WAIT does not consume bus cycles once the queue is full.

If a local bus request occurs during WAIT execution, the 8088 3-states all output drivers. If interrupts are enabled, the 8088 will recognize interrupts and process them. The WAIT instruction is then refetched, and reexecuted.

Basic System Timing

In minimum mode, the MN/$\overline{MX}$ pin is strapped to V_{CC} and the processor emits bus control signals compatible with the 8085 bus structure. In maximum mode, the MN/$\overline{MX}$ pin is strapped to GND and the processor emits coded status information which the 8288 bus controller uses to generate MULTIBUS compatible bus control signals.

System Timing — Minimum System

(See Figure 8.)

The read cycle begins in T1 with the assertion of the address latch enable (ALE) signal. The trailing (low going) edge of this signal is used to latch the address information, which is valid on the address/data bus (AD0–AD7) at this time, into the 8282/8283 latch. Address lines A8 through A15 do not need to be latched because they remain valid throughout the bus cycle. From T1 to T4 the IO/$\overline{M}$ signal indicates a memory or I/O operation. At T2 the address is removed from the address/data bus and the bus goes to a high impedance state. The read control signal is also asserted at T2. The read ($\overline{RD}$) signal causes the addressed device to enable its data bus drivers to the local bus. Some time later, valid data will be available on the bus and the addressed device will drive the READY line HIGH. When the processor returns the read signal to a HIGH level, the addressed device will again 3-state its bus drivers. If a transceiver (8286/8287) is required to buffer the 8088 local bus, signals DT/$\overline{R}$ and $\overline{DEN}$ are provided by the 8088.

A write cycle also begins with the assertion of ALE and the emission of the address. The IO/$\overline{M}$ signal is again asserted to indicate a memory or I/O write operation. In T2, immediately following the address emission, the processor emits the data to be written into the addressed location. This data remains valid until at least the middle of T4. During T2, T3, and T_W, the processor asserts the write control signal. The write ($\overline{WR}$) signal becomes active at the beginning of T2, as opposed to the read, which is delayed somewhat into T2 to provide time for the bus to float.

The basic difference between the interrupt acknowledge cycle and a read cycle is that the interrupt acknowledge ($\overline{INTA}$) signal is asserted in place of the read ($\overline{RD}$) signal and the address bus is floated. (See Figure 9.) In the second of two successive $\overline{INTA}$ cycles, a byte of information is read from the data bus, as supplied by the interrupt system logic (i.e. 8259A priority interrupt controller). This byte identifies the source (type) of the interrupt. It is multiplied by four and used as a pointer into the interrupt vector lookup table, as described earlier.

Bus Timing — Medium Complexity Systems

(See Figure 10.)

For medium complexity systems, the MN/$\overline{MX}$ pin is connected to GND and the 8288 bus controller is added to the system, as well as an 8282/8283 latch for latching the system address, and an 8286/8287 transceiver to allow for bus loading greater than the 8088 is capable of handling. Signals ALE, $\overline{DEN}$, and DT/$\overline{R}$ are generated by the 8288 instead of the processor in this configuration, although their timing remains relatively the same. The 8088 status outputs ($\overline{S2}$, $\overline{S1}$, and $\overline{S0}$) provide type of cycle information and become 8288 inputs. This bus cycle information specifies read (code, data, or I/O), write (data or I/O), interrupt acknowledge, or software halt. The 8288 thus issues control signals specifying memory read or write, I/O read or write, or interrupt acknowledge. The 8288 provides two types of write strobes, normal and advanced, to be applied as required. The normal write strobes have data valid at the leading edge of write. The advanced write strobes have the same timing as read strobes, and hence, data is not valid at the leading edge of write. The 8286/8287 transceiver receives the usual T and $\overline{OE}$ inputs from the 8288's DT/$\overline{R}$ and $\overline{DEN}$ outputs.

The pointer into the interrupt vector table, which is passed during the second $\overline{INTA}$ cycle, can derive from an 8259A located on either the local bus or the system bus. If the master 8289A priority interrupt controller is positioned on the local bus, a TTL gate is required to disable the 8286/8287 transceiver when reading from the master 8259A during the interrupt acknowledge sequence and software "poll".

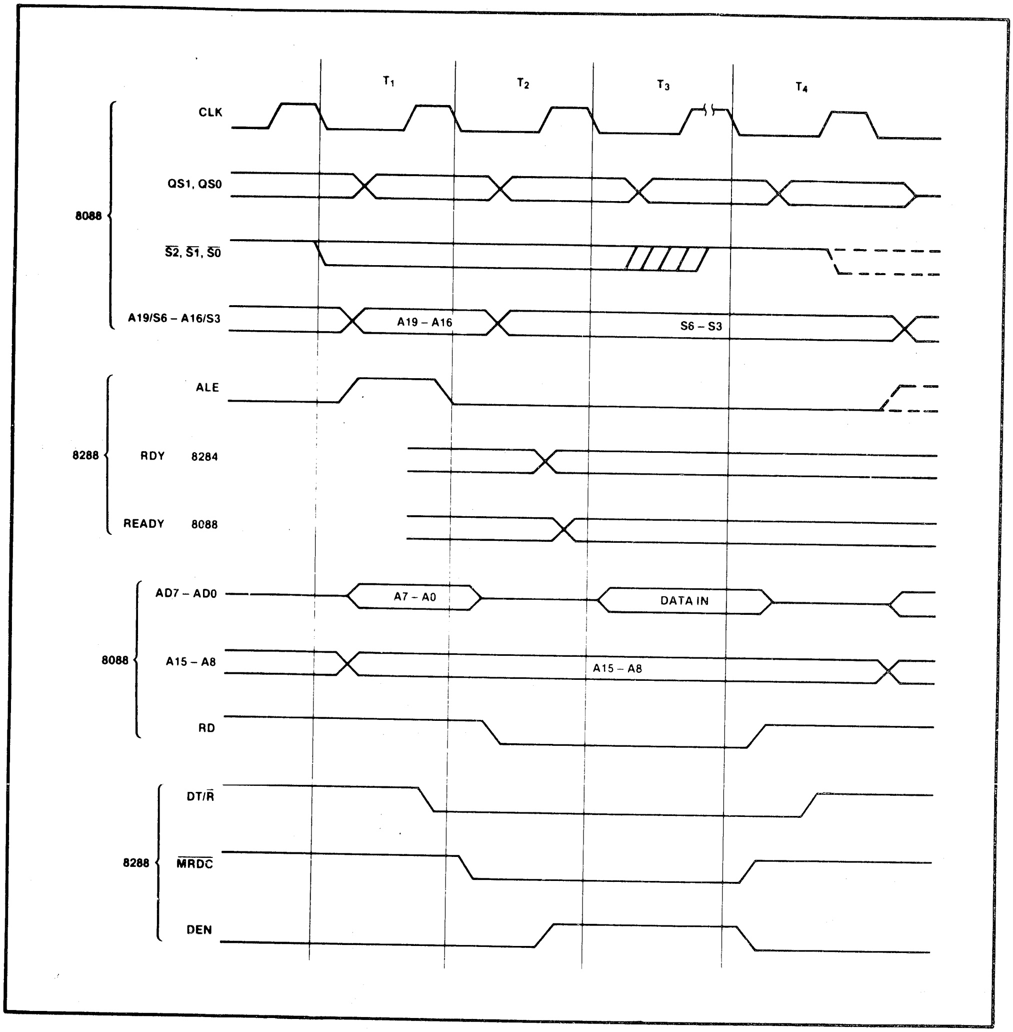


Figure 10. Medium Complexity System Timing

The 8088 Compared to the 8086

The 8088 CPU is an 8-bit processor designed around the 8086 internal structure. Most internal functions of the 8088 are identical to the equivalent 8086 functions. The 8088 handles the external bus the same way the 8086 does with the distinction of handling only 8 bits at a time. Sixteen-bit operands are fetched or written in two consecutive bus cycles. Both processors will appear identical to the software engineer, with the exception of execution time. The internal register structure is identical and all instructions have the same end result. The differences between the 8088 and 8086 are outlined below. The engineer who is unfamiliar with the 8086 is referred to the iAPX 86, 88 User's Manual, Chapters 2 and 4, for function description and instruction set information. Internally, there are three differences between the 8088 and the 8086. All changes are related to the 8-bit bus interface.

- The queue length is 4 bytes in the 8088, whereas the 8086 queue contains 6 bytes, or three words. The queue was shortened to prevent overuse of the bus by the BIU when prefetching instructions. This was required because of the additional time necessary to fetch instructions 8 bits at a time.
- To further optimize the queue, the prefetching algorithm was changed. The 8088 BIU will fetch a new instruction to load into the queue each time there is a 1 byte hole (space available) in the queue. The 8086 waits until a 2-byte space is available.
- The internal execution time of the instruction set is affected by the 8-bit interface. All 16-bit fetches and writes from/to memory take an additional four clock cycles. The CPU is also limited by the speed of instruction fetches. This latter problem only occurs when a series of simple operations occur. When the more sophisticated instructions of the 8088 are being used, the queue has time to fill and the execution proceeds as fast as the execution unit will allow.

The 8088 and 8086 are completely software compatible by virture of their identical execution units. Software that is system dependent may not be completely transferable, but software that is not system dependent will operate equally as well on an 8088 or an 8086.

The hardware interface of the 8088 contains the major differences between the two CPUs. The pin assignments are nearly identical, however, with the following functional changes:

- A8–A15 — These pins are only address outputs on the 8088. These address lines are latched internally and remain valid throughout a bus cycle in a manner similar to the 8085 upper address lines.
- $\overline{\text{BHE}}$ has no meaning on the 8088 and has been eliminated.
- $\overline{\text{SSO}}$ provides the $\overline{\text{SO}}$ status information in the minimum mode. This output occurs on pin 34 in minimum mode only. DT/$\overline{\text{R}}$, IO/$\overline{\text{M}}$, and $\overline{\text{SSO}}$ provide the complete bus status in minimum mode.
- IO/$\overline{\text{M}}$ has been inverted to be compatible with the MCS-85 bus structure.
- ALE is delayed by one clock cycle in the minimum mode when entering HALT, to allow the status to be latched with ALE.

D-8088 P-8088

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ....0 °C to 70 °C
Storage Temperature .... − 65 °C to + 150 °C
Voltage on Any Pin with
Respect to Ground .... - 1.0 to + 7V
Power Dissipation .... 2.5 Watt

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

(8088: T_A = 0°C to 70°C, V_{CC} = 5V ±10%) (5 MHz)
(8088-2: T_A = 0°C to 70°C, V_{CC} = 5V ±5%) (8 MHz)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
I_{CC}	Power Supply Current: 8088 8088-2		340 350	mA	T_A = 25°C
I_{LI}	Input Leakage Current		±10	μA	0V ≤ V_{IN} ≤ V_{CC}
I_{LO}	Output Leakage Current		±10	μA	0.45V ≤ V_{OUT} ≤ V_{CC}
V_{CL}	Clock Input Low Voltage	−0.5	+0.6	V	
V_{CH}	Clock Input High Voltage	3.9	V_{CC}+1.0	V	
C_{IN}	Capacitance if Input Buffer (All input except AD_0-AD_7, $\overline{RQ}/\overline{GT}$		15	pF	fc = 1 MHz
C_{IO}	Capacitance of I/O Buffer (AD_0-AD_7, $\overline{RQ}/\overline{GT}$		15	pF	fc = 1 MHz

5

A.C. CHARACTERISTICS (8088: T_A = 0°C to 70°C, V_{CC} = 5V ±10%) (5 MHz) (8088-2: T_A = 0°C to 70°C, V_{CC} = 5V ±5%) (8 MHz)

MINIMUM COMPLEXITY SYSTEM TIMING REQUIREMENTS

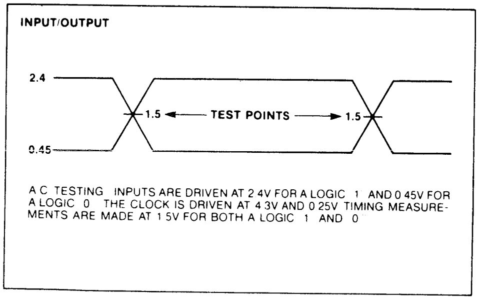
		8088 (5 MHz)		8088-2 (8 MHz)			
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**	**Test Conditions**
TCLCL	CLK Cycle Period	200	500	125	500	ns	
TCLCH	CLK Low Time	(⅔ TCLCL)−15		(⅔ TCLCL)−15		ns	
TCHCL	CLK High Time	(⅓ TCLCL)+2		(⅓ TCLCL)+2		ns	
TCH1CH2	CLK Rise Time		10		10	ns	From 1.0V to 3.5V
TCL2CL1	CLK Fall Time		10		10	ns	From 3.5V to 1.0V
TDVCL	Data in Setup Time	30		20		ns	
TCLDX	Data in Hold Time	10		10		ns	
TR1VCL	RDY Setup Time into 8284 (See Notes 1, 2)	35		35		ns	
TCLR1X	RDY Hold Time into 8284 (See Notes 1, 2)	0		0		ns	
TRYHCH	READY Setup Time into 8088	(⅔ TCLCL)−15		(⅔ TCLCL)−15		ns	
TCHRYX	READY Hold Time into 8088	30		20		ns	
TRYLCL	READY Inactive to CLK (See Note 3)	−8		−8		ns	
THVCH	HOLD Setup Time	35		20		ns	
TINVCH	INTR, NMI, $\overline{\text{TEST}}$ Setup Time (See Note 2)	30		15		ns	
TILIH	Input Rise Time (Except CLK)		20		20	ns	From 0.8V to 2.0V
TIHIL	Input Fall Time (Except CLK)		12		12	ns	From 2.0V to 0.8V

A.C. CHARACTERISTICS (Continued)

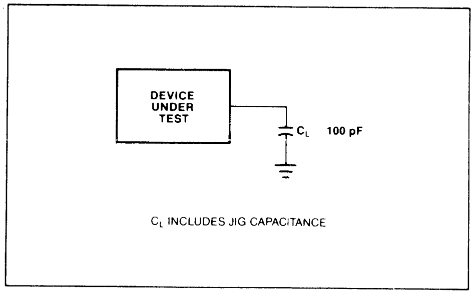
TIMING RESPONSES

Symbol	Parameter	8088 (5 MHz) Min.	8088 (5 MHz) Max.	8088-2 (8 MHz) Min.	8088-2 (8 MHz) Max.	Units	Test Conditions
TCLAV	Address Valid Delay	10	110	10	60	ns	
TCLAX	Address Hold Time	10		10		ns	
TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50	ns	
TLHLL	ALE Width	TCLCH−20		TCLCH−10		ns	
TCLLH	ALE Active Delay		80		50	ns	
TCHLL	ALE Inactive Delay		85		55	ns	
TLLAX	Address Hold Time to ALE Inactive	TCHCL−10		TCHCL−10		ns	
TCLDV	Data Valid Delay	10	110	10	60	ns	C_L = 20-100 pF for all 8088 Outputs in addition to internal loads
TCHDX	Data Hold Time	10		10		ns	
TWHDX	Data Hold Time After $\overline{WR}$	TCLCH−30		TCLCH−30		ns	
TCVCTV	Control Active Delay 1	10	110	10	70	ns	
TCHCTV	Control Active Delay 2	10	110	10	60	ns	
TCVCTX	Control Inactive Delay	10	110	10	70	ns	
TAZRL	Address Float to READ Active	0		0		ns	
TCLRL	$\overline{RD}$ Active Delay	10	165	10	100	ns	
TCLRH	$\overline{RD}$ Inactive Delay	10	150	10	80	ns	
TRHAV	$\overline{RD}$ Inactive to Next Address Active	TCLCL−45		TCLCL−40		ns	
TCLHAV	HLDA Valid Delay	10	160	10	100	ns	
TRLRH	$\overline{RD}$ Width	2TCLCL−75		2TCLCL−50		ns	
TWLWH	$\overline{WR}$ Width	2TCLCL−60		2TCLCL−40		ns	
TAVAL	Address Valid to ALE Low	TCLCH−60		TCLCH−40		ns	
TOLOH	Output Rise Time		20		20	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		12		12	ns	From 2.0V to 0.8V

A.C. TESTING INPUT, OUTPUT WAVEFORM

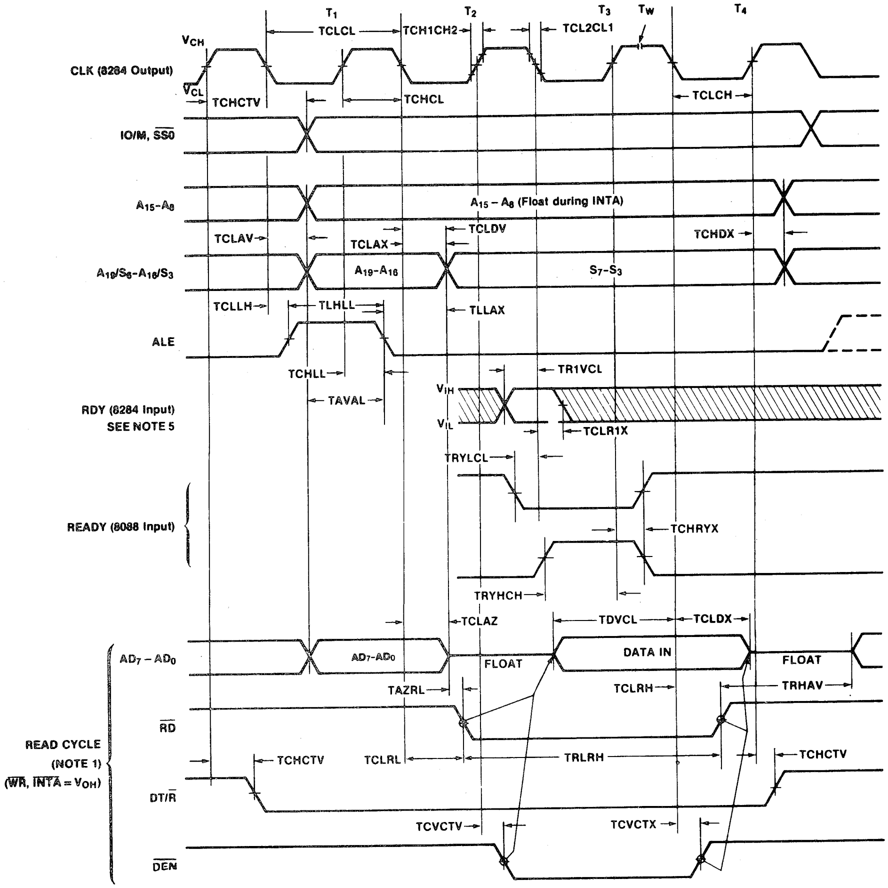


A.C. TESTING LOAD CIRCUIT



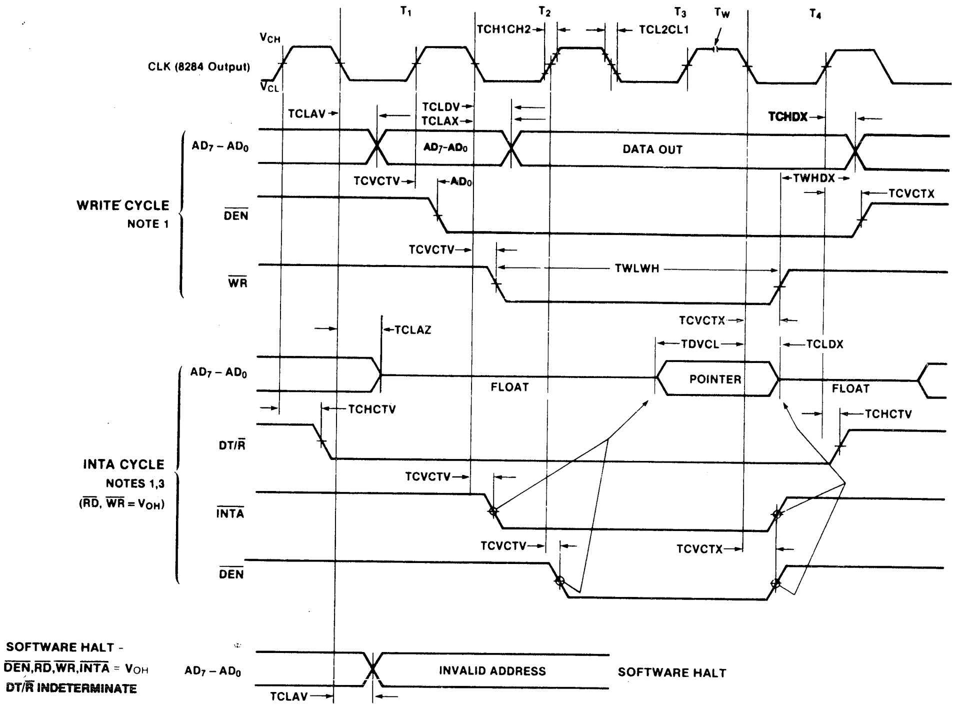
WAVEFORMS

BUS TIMING—MINIMUM MODE SYSTEM



WAVEFORMS (Continued)

BUS TIMING—MINIMUM MODE SYSTEM (Continued)



NOTES:
1. ALL SIGNALS SWITCH BETWEEN V_{OH} AND V_{OL} UNLESS OTHERWISE SPECIFIED.
2. RDY IS SAMPLED NEAR THE END OF T_2, T_3, T_W TO DETERMINE IF T_W MACHINES STATES ARE TO BE INSERTED.
3. TWO INTA CYCLES RUN BACK-TO-BACK. THE 8088 LOCAL ADDR/DATA BUS IS FLOATING DURING BOTH INTA CYCLES. CONTROL SIGNALS ARE SHOWN FOR THE SECOND INTA CYCLE.
4. SIGNALS AT 8284 ARE SHOWN FOR REFERENCE ONLY.
5. ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS OTHERWISE NOTED.

A.C. CHARACTERISTICS

MAX MODE SYSTEM (USING 8288 BUS CONTROLLER)
TIMING REQUIREMENTS

Symbol	Parameter	8088 (5 MHz) Min.	8088 (5 MHz) Max.	8088-2 (8 MHz) Min.	8088-2 (8 MHz) Max.	Units	Test Conditions
TCLCL	CLK Cycle Period	200	500	125	500	ns	
TCLCH	CLK Low Time	(⅔TCLCL) − 15		(⅔TCLCL) − 15		ns	
TCHCL	CLK High Time	(⅓TCLCL) + 2		(⅓TCLCL) + 2		ns	
TCH1CH2	CLK Rise Time		10		10	ns	From 1.0V to 3.5V
TCL2CL1	CLK Fall Time		10		10	ns	From 3.5V to 1.0V
TDVCL	Data In Setup Time	30		20		ns	
TCLDX	Data In Hold Time	10		10		ns	
TR1VCL	RDY Setup Time into 8284 (See Notes 1, 2)	35		35		ns	
TCLR1X	RDY Hold Time into 8284 (See Notes 1, 2)	0		0		ns	
TRYHCH	READY Setup Time into 8088	(⅔TCLCL) − 15		(⅔TCLCL) − 15		ns	
TCHRYX	READY Hold Time into 8088	30		20		ns	
TRYLCL	READY Inactive to CLK (See Note 4)	−8		−8		ns	
TINVCH	Setup Time for Recognition (INTR, NMI, TEST) (See Note 2)	30		15		ns	
TGVCH	RQ/GT Setup Time	30		15		ns	
TCHGX	RQ Hold Time into 8086	40		30		ns	
TILIH	Input Rise Time (Except CLK)		20		20	ns	From 0.8V to 2.0V
TIHIL	Input Fall Time (Except CLK)		12		12	ns	From 2.0V to 0.8V

NOTES:
1. Signal at 8284 or 8288 shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T2 state (8 ns into T3 state).
4. Applies only to T2 state (8 ns into T3 state).

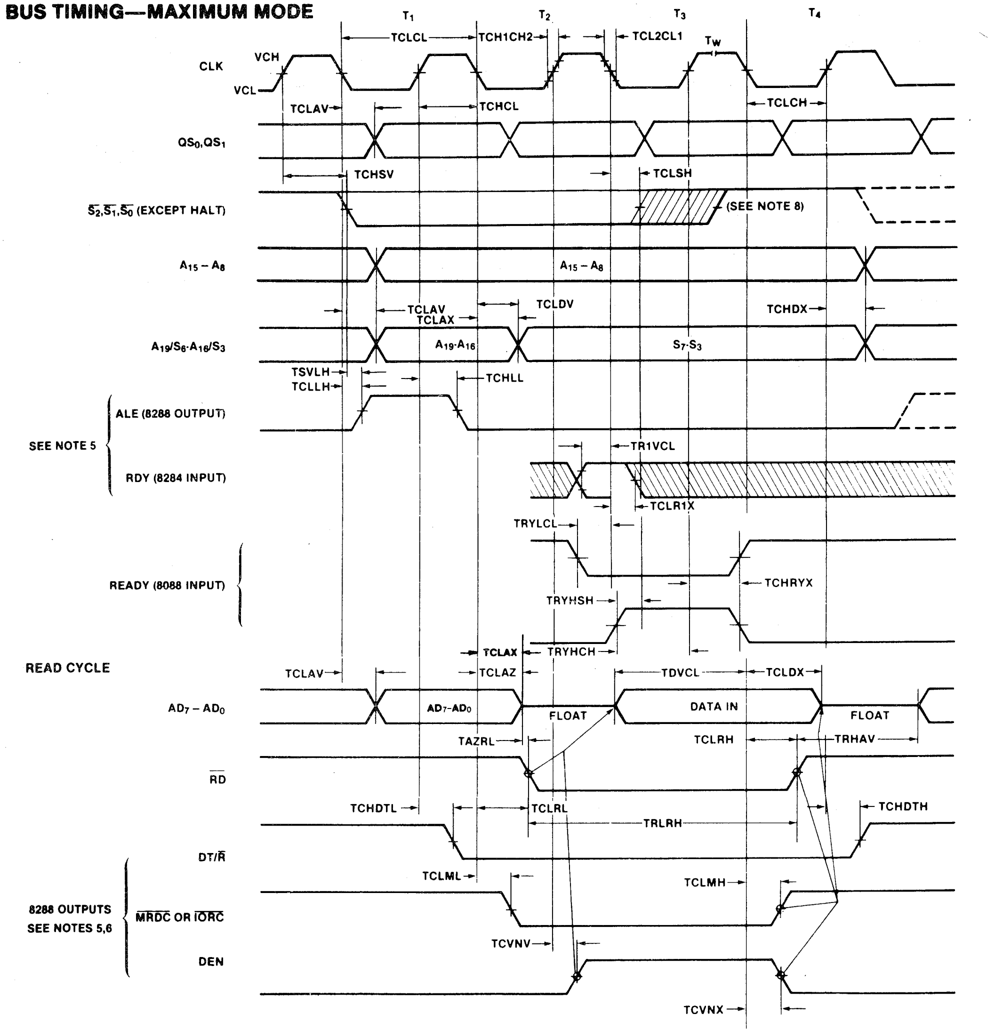
A.C. CHARACTERISTICS (Continued)

TIMING RESPONSES

Symbol	Parameter	8088 (5 MHz) Min.	8088 (5 MHz) Max.	8088-2 (8 MHz) Min.	8088-2 (8 MHz) Max.	Units	Test Conditions
TCLML	Command Active Delay (See Note 1)	10	35	10	35	ns	
TCLMH	Command Inactive Delay (See Note 1)	10	35	10	35	ns	
TRYHSH	READY Active to Status Passive (See Note 3)		110		65	ns	
TCHSV	Status Active Delay	10	110	10	60	ns	
TCLSH	Status Inactive Delay	10	130	10	70	ns	
TCLAV	Address Valid Delay	10	110	10	60	ns	
TCLAX	Address Hold Time	10		10		ns	C_L = 20-100 pF for all 8088 Outputs in addition to internal loads
TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50	ns	
TSVLH	Status Valid to ALE High (See Note 1)		15		15	ns	
TSVMCH	Status Valid to MCE High (See Note 1)		15		15	ns	
TCLLH	CLK Low to ALE Valid (See Note 1)		15		15	ns	
TCLMCH	CLK Low to MCE High (See Note 1)		15		15	ns	
TCHLL	ALE Inactive Delay (See Note 1)		15		15	ns	
TCLMCL	MCE Inactive Delay (See Note 1)		15		15	ns	
TCLDV	Data Valid Delay	10	110	10	60	ns	
TCHDX	Data Hold Time	10		10		ns	
TCVNV	Control Active Delay (See Note 1)	5	45	5	45	ns	
TCVNX	Control Inactive Delay (See Note 1)	10	45	10	45	ns	
TAZRL	Address Float to Read Active	0		0		ns	
TCLRL	RD Active Delay	10	165	10	100	ns	
TCLRH	RD Inactive Delay	10	150	10	80	ns	
TRHAV	RD Inactive to Next Address Active	TCLCL−45		TCLCL−40		ns	
TCHDTL	Direction Control Active Delay (See Note 1)		50		50	ns	
TCHDTH	Direction Control Inactive Delay (See Note 1)		30		30	ns	
TCLGL	GT Active Delay		85		50	ns	
TCLGH	GT Inactive Delay		85		50	ns	
TRLRH	RD Width	2TCLCL−75		2TCLCL−50		ns	
TOLOH	Output Rise Time		20		20	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		12		12	ns	From 2.0V to 0.8V

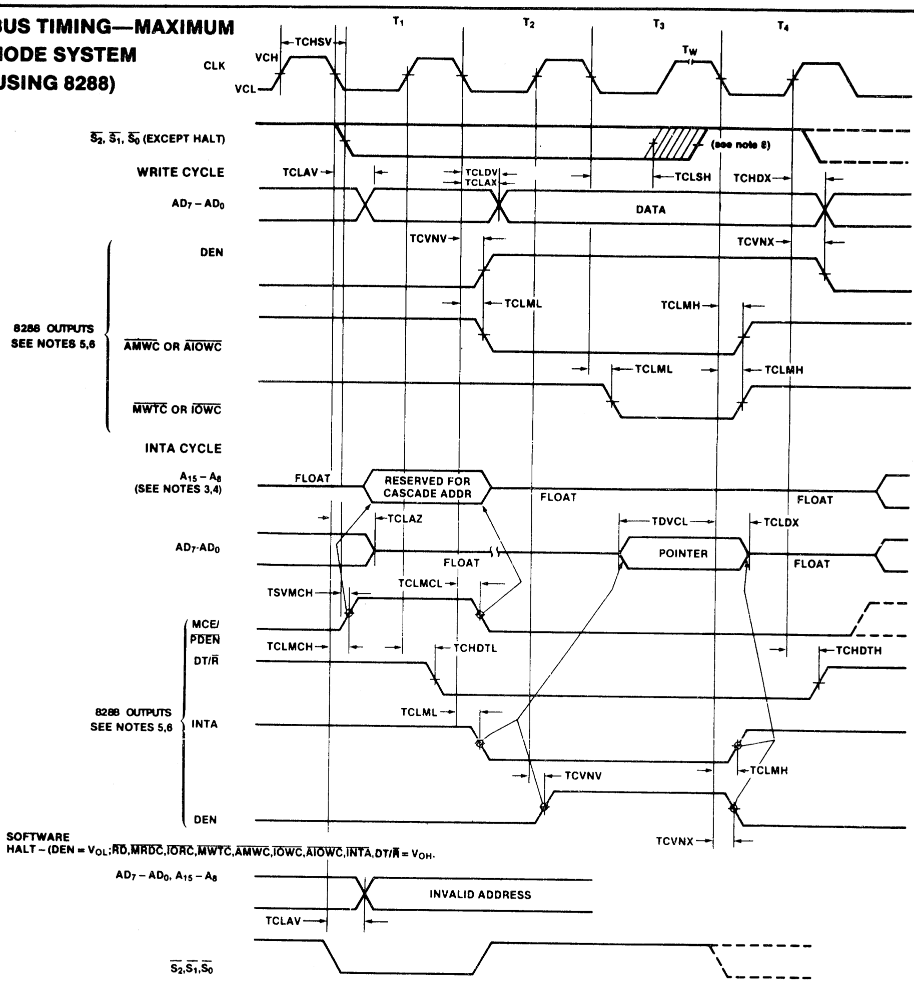
WAVEFORMS

BUS TIMING—MAXIMUM MODE



WAVEFORMS (Continued)

BUS TIMING—MAXIMUM MODE SYSTEM (USING 8288)

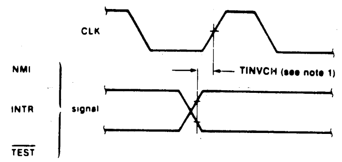


NOTES:

1. ALL SIGNALS SWITCH BETWEEN V_{OH} AND V_{OL} UNLESS OTHERWISE SPECIFIED.
2. RDY IS SAMPLED NEAR THE END OF T_2, T_3, T_W TO DETERMINE IF T_W MACHINES STATES ARE TO BE INSERTED.
3. CASCADE ADDRESS IS VALID BETWEEN FIRST AND SECOND INTA CYCLES.
4. TWO INTA CYCLES RUN BACK-TO-BACK. THE 8088 LOCAL ADDR/DATA BUS IS FLOATING DURING BOTH INTA CYCLES. CONTROL FOR POINTER ADDRESS IS SHOWN FOR SECOND INTA CYCLE.
5. SIGNALS AT 8284 OR 8288 ARE SHOWN FOR REFERENCE ONLY.
6. THE ISSUANCE OF THE 8288 COMMAND AND CONTROL SIGNALS ($\overline{MRDC}$, $\overline{MWTC}$, $\overline{AMWC}$, $\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$ AND DEN) LAGS THE ACTIVE HIGH 8288 CEN.
7. ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS OTHERWISE NOTED.
8. STATUS INACTIVE IN STATE JUST PRIOR TO T_4.

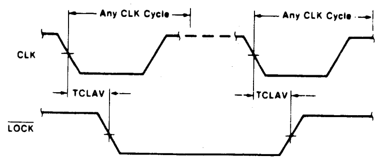
WAVEFORMS (Continued)

ASYNCHRONOUS SIGNAL RECOGNITION

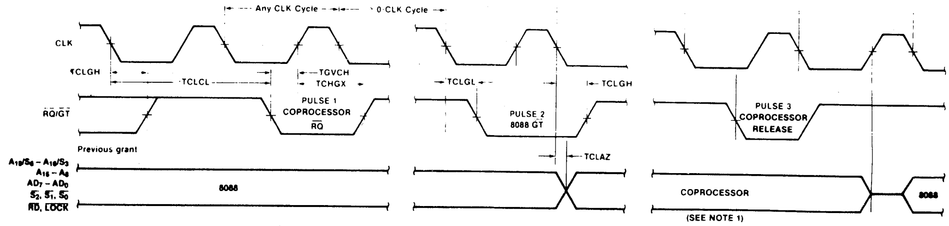


NOTE: 1. SETUP REQUIREMENTS FOR ASYNCHRONOUS SIGNALS ONLY TO GUARANTEE RECOGNITION AT NEXT CLK

BUS LOCK SIGNAL TIMING (MAXIMUM MODE ONLY)

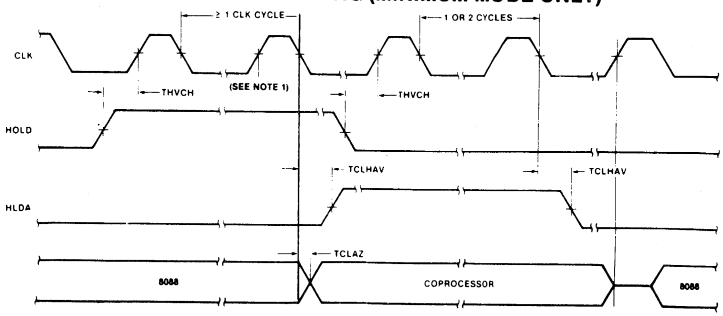


REQUEST/GRANT SEQUENCE TIMING (MAXIMUM MODE ONLY)



NOTE: 1. THE COPROCESSOR MAY NOT DRIVE THE BUSSES OUTSIDE THE REGION SHOWN WITHOUT RISKING CONTENTION.

HOLD/HOLD ACKNOWLEDGE TIMING (MINIMUM MODE ONLY)



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8086 - 8088

INSTRUCTION SET SUMMARY

DATA TRANSFER

MOV = **Move**:	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Register/memory to/from register	1 0 0 0 1 0 d w	mod reg r/m		
Immediate to register/memory	1 1 0 0 0 1 1 w	mod 0 0 0 r/m	data	data if w 1
Immediate to register	1 0 1 1 w reg	data	data if w 1	
Memory to accumulator	1 0 1 0 0 0 0 w	addr-low	addr-high	
Accumulator to memory	1 0 1 0 0 0 1 w	addr-low	addr-high	
Register/memory to segment register	1 0 0 0 1 1 1 0	mod 0 reg r/m		
Segment register to register/memory	1 0 0 0 1 1 0 0	mod 0 reg r/m		

PUSH = **Push**:		
Register/memory	1 1 1 1 1 1 1 1	mod 1 1 0 r/m
Register	0 1 0 1 0 reg	
Segment register	0 0 0 reg 1 1 0	

POP = **Pop**:		
Register/memory	1 0 0 0 1 1 1 1	mod 0 0 0 r/m
Register	0 1 0 1 1 reg	
Segment register	0 0 0 reg 1 1 1	

XCHG = **Exchange**:		
Register/memory with register	1 0 0 0 0 1 1 w	mod reg r/m
Register with accumulator	1 0 0 1 0 reg	

IN=Input from		
Fixed port	1 1 1 0 0 1 0 w	port
Variable port	1 1 1 0 1 1 0 w	

OUT = Output to		
Fixed port	1 1 1 0 0 1 1 w	port
Variable port	1 1 1 0 1 1 1 w	
XLAT=Translate byte to AL	1 1 0 1 0 1 1 1	
LEA=Load EA to register	1 0 0 0 1 1 0 1	mod reg r/m
LDS=Load pointer to DS	1 1 0 0 0 1 0 1	mod reg r/m
LES=Load pointer to ES	1 1 0 0 0 1 0 0	mod reg r/m
LAHF=Load AH with flags	1 0 0 1 1 1 1 1	
SAHF=Store AH into flags	1 0 0 1 1 1 1 0	
PUSHF=Push flags	1 0 0 1 1 1 0 0	
POPF=Pop flags	1 0 0 1 1 1 0 1	

ARITHMETIC

ADD = **Add**:				
Reg./memory with register to either	0 0 0 0 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 s w	mod 0 0 0 r/m	data	data if s w 01
Immediate to accumulator	0 0 0 0 0 1 0 w	data	data if w 1	

ADC = **Add with carry**:				
Reg./memory with register to either	0 0 0 1 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 s w	mod 0 1 0 r/m	data	data if s w 01
Immediate to accumulator	0 0 0 1 0 1 0 w	data	data if w 1	

INC = **Increment**:		
Register/memory	1 1 1 1 1 1 1 w	mod 0 0 0 r/m
Register	0 1 0 0 0 reg	
AAA=ASCII adjust for add	0 0 1 1 0 1 1 1	
DAA=Decimal adjust for add	0 0 1 0 0 1 1 1	

SUB = **Subtract**:				
Reg./memory and register to either	0 0 1 0 1 0 d w	mod reg r/m		
Immediate from register/memory	1 0 0 0 0 0 s w	mod 1 0 1 r/m	data	data if s w 01
Immediate from accumulator	0 0 1 0 1 1 0 w	data	data if w 1	

SBB = **Subtract with borrow**				
Reg./memory and register to either	0 0 0 1 1 0 d w	mod reg r/m		
Immediate from register/memory	1 0 0 0 0 0 s w	mod 0 1 1 r/m	data	data if s w 01
Immediate from accumulator	0 0 0 1 1 1 0 w	data	data if w 1	

DEC = **Decrement**:	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Register/memory	1 1 1 1 1 1 1 w	mod 0 0 1 r/m		
Register	0 1 0 0 1 reg			
NEG Change sign	1 1 1 1 0 1 1 w	mod 0 1 1 r/m		

CMP = **Compare**:				
Register/memory and register	0 0 1 1 1 0 d w	mod reg r/m		
Immediate with register/memory	1 0 0 0 0 0 s w	mod 1 1 1 r/m	data	data if s w 01
Immediate with accumulator	0 0 1 1 1 1 0 w	data	data if w 1	
AAS ASCII adjust for subtract	0 0 1 1 1 1 1 1			
DAS Decimal adjust for subtract	0 0 1 0 1 1 1 1			
MUL Multiply (unsigned)	1 1 1 1 0 1 1 w	mod 1 0 0 r/m		
IMUL Integer multiply (signed)	1 1 1 1 0 1 1 w	mod 1 0 1 r/m		
AAM ASCII adjust for multiply	1 1 0 1 0 1 0 0	0 0 0 0 1 0 1 0		
DIV Divide (unsigned)	1 1 1 1 0 1 1 w	mod 1 1 0 r/m		
IDIV Integer divide (signed)	1 1 1 1 0 1 1 w	mod 1 1 1 r/m		
AAD ASCII adjust for divide	1 1 0 1 0 1 0 1	0 0 0 0 1 0 1 0		
CBW Convert byte to word	1 0 0 1 1 0 0 0			
CWD Convert word to double word	1 0 0 1 1 0 0 1			

LOGIC

NOT Invert	1 1 1 1 0 1 1 w	mod 0 1 0 r/m
SHL/SAL Shift logical/arithmetic left	1 1 0 1 0 0 v w	mod 1 0 0 r/m
SHR Shift logical right	1 1 0 1 0 0 v w	mod 1 0 1 r/m
SAR Shift arithmetic right	1 1 0 1 0 0 v w	mod 1 1 1 r/m
ROL Rotate left	1 1 0 1 0 0 v w	mod 0 0 0 r/m
ROR Rotate right	1 1 0 1 0 0 v w	mod 0 0 1 r/m
RCL Rotate through carry flag left	1 1 0 1 0 0 v w	mod 0 1 0 r/m
RCR Rotate through carry right	1 1 0 1 0 0 v w	mod 0 1 1 r/m

AND = **And**:				
Reg./memory and register to either	0 0 1 0 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 0 0 r/m	data	data if w 1
Immediate to accumulator	0 0 1 0 0 1 0 w	data	data if w 1	

TEST = **And function to flags, no result**:				
Register/memory and register	1 0 0 0 0 1 0 w	mod reg r/m		
Immediate data and register/memory	1 1 1 1 0 1 1 w	mod 0 0 0 r/m	data	data if w 1
Immediate data and accumulator	1 0 1 0 1 0 0 w	data	data if w 1	

OR = **Or**:				
Reg./memory and register to either	0 0 0 0 1 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 0 0 1 r/m	data	data if w 1
Immediate to accumulator	0 0 0 0 1 1 0 w	data	data if w 1	

XOR = **Exclusive or**:				
Reg./memory and register to either	0 0 1 1 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 1 0 r/m	data	data if w 1
Immediate to accumulator	0 0 1 1 0 1 0 w	data	data if w 1	

STRING MANIPULATION

REP=Repeat	1 1 1 1 0 0 1 z
MOVS=Move byte/word	1 0 1 0 0 1 0 w
CMPS=Compare byte/word	1 0 1 0 0 1 1 w
SCAS=Scan byte/word	1 0 1 0 1 1 1 w
LODS=Load byte/wd to AL/AX	1 0 1 0 1 1 0 w
STOS=Stor byte/wd from AL/A	1 0 1 0 1 0 1 w

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INSTRUCTION SET SUMMARY (Continued)

CONTROL TRANSFER

CALL = Call:

	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Direct within segment	1 1 1 0 1 0 0 0	disp-low	disp-high
Indirect within segment	1 1 1 1 1 1 1 1	mod 0 1 0 r/m	
Direct intersegment	1 0 0 1 1 0 1 0	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	1 1 1 1 1 1 1 1	mod 0 1 1 r/m	

JMP = Unconditional Jump:

Direct within segment	1 1 1 0 1 0 0 1	disp-low	disp-high
Direct within segment-short	1 1 1 0 1 0 1 1	disp	
Indirect within segment	1 1 1 1 1 1 1 1	mod 1 0 0 r/m	
Direct intersegment	1 1 1 0 1 0 1 0	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	1 1 1 1 1 1 1 1	mod 1 0 1 r/m	

RET = Return from CALL:

Within segment	1 1 0 0 0 0 1 1		
Within seg adding immed to SP	1 1 0 0 0 0 1 0	data-low	data-high
Intersegment	1 1 0 0 1 0 1 1		
Intersegment, adding immediate to SP	1 1 0 0 1 0 1 0	data-low	data-high
JE/JZ = Jump on equal/zero	0 1 1 1 0 1 0 0	disp	
JL/JNGE = Jump on less/not greater or equal	0 1 1 1 1 1 0 0	disp	
JLE/JNG = Jump on less or equal/not greater	0 1 1 1 1 1 1 0	disp	
JB/JNAE = Jump on below/not above or equal	0 1 1 1 0 0 1 0	disp	
JBE/JNA = Jump on below or equal/not above	0 1 1 1 0 1 1 0	disp	
JP/JPE = Jump on parity/parity even	0 1 1 1 1 0 1 0	disp	
JO = Jump on overflow	0 1 1 1 0 0 0 0	disp	
JS = Jump on sign	0 1 1 1 1 0 0 0	disp	
JNE/JNZ = Jump on not equal/not zero	0 1 1 1 0 1 0 1	disp	
JNL/JGE = Jump on not less/greater or equal	0 1 1 1 1 1 0 1	disp	
JNLE/JG = Jump on not less or equal/greater	0 1 1 1 1 1 1 1	disp	

	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
JNB/JAE Jump on not below/above or equal	0 1 1 1 0 0 1 1	disp
JNBE/JA Jump on not below or equal/above	0 1 1 1 0 1 1 1	disp
JNP/JPO Jump on not par/par odd	0 1 1 1 1 0 1 1	disp
JNO Jump on not overflow	0 1 1 1 0 0 0 1	disp
JNS Jump on not sign	0 1 1 1 1 0 0 1	disp
LOOP Loop CX times	1 1 1 0 0 0 1 0	disp
LOOPZ/LOOPE Loop while zero/equal	1 1 1 0 0 0 0 1	disp
LOOPNZ/LOOPNE Loop while not zero/equal	1 1 1 0 0 0 0 0	disp
JCXZ Jump on CX zero	1 1 1 0 0 0 1 1	disp

INT Interrupt

Type specified	1 1 0 0 1 1 0 1	type
Type 3	1 1 0 0 1 1 0 0	
INTO Interrupt on overflow	1 1 0 0 1 1 1 0	
IRET Interrupt return	1 1 0 0 1 1 1 1	

PROCESSOR CONTROL

CLC Clear carry	1 1 1 1 1 0 0 0	
CMC Complement carry	1 1 1 1 0 1 0 1	
STC Set carry	1 1 1 1 1 0 0 1	
CLD Clear direction	1 1 1 1 1 1 0 0	
STD Set direction	1 1 1 1 1 1 0 1	
CLI Clear interrupt	1 1 1 1 1 0 1 0	
STI Set interrupt	1 1 1 1 1 0 1 1	
HLT Halt	1 1 1 1 0 1 0 0	
WAIT Wait	1 0 0 1 1 0 1 1	
ESC Escape (to external device)	1 1 0 1 1 x x x	mod x x x r/m
LOCK Bus lock prefix	1 1 1 1 0 0 0 0	

Footnotes:

AL = 8-bit accumulator
AX = 16-bit accumulator
CX = Count register
DS = Data segment
ES = Extra segment
Above/below refers to unsigned value.
Greater = more positive;
Less = less positive (more negative) signed values
if d = 1 then "to" reg; if d = 0 then "from" reg
if w = 1 then word instruction; if w = 0 then byte instruction

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low

if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP
DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

if s:w = 01 then 16 bits of immediate data form the operand
if s:w = 11 then an immediate data byte is sign extended to form the 16-bit operand
if v = 0 then "count" = 1; if v = 1 then "count" in (CL)
x = don't care
z is used for string primitives for comparison with ZF FLAG

SEGMENT OVERRIDE PREFIX

0 0 1 reg 1 1 0

REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)	Segment
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	
101 BP	101 CH	
110 SI	110 DH	
111 DI	111 BH	

Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:

FLAGS = X:X:X:X:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

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ORDERING INFORMATION

Part number	Temperature range	Freq. (MHz)	Vcc (V)	Package
D-8088 P-8088	commercial 0° - 70° C	5	5 V ± 10 %	cerdip plastic
D-8088-2 P-8088-2	0° - 70° C	8	5 V ± 5 %	cerdip plastic

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Microprocessor support system 6

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Introduction

Datasheets and databooks provide the first bits of information needed to understand the function of an integrated circuit. The user finds information such as : circuit features, pin-out, power consumption and timing diagrams. Quite often however this is not enough to correctly use an integrated circuit.

Once you wish to design - in a product, you almost always need more detailed information than that given in the datasheet. This is especially true for microprocessor-, memory-, and peripheral circuits, where instruction sets and timing are extremely important aspects of a system, and where circuit complexity increases the need of more detailed and in - depth data. Information like this is obtained either by asking competent engineers who know the circuit very well, due to the fact that they have used the circuit before, or by consulting Application Notes having a common point with the application in question.

The user needs this information to successfully use any type of integrated circuit.

Due to this kind of demand, full Technical Support is a necessary and a very important service that the semiconductor manufacturer offers to its customers.

Matra-Harris technical support group

MHS has created a technical support group capable of giving full support, both to its customers and to the MHS product design group, as can be seen in the block diagram on the next page.

The MHS technical support group has three functions :

Customer support

i) The primary role of this function is Customer Aid. This means that customers can rely on receiving complete and accurate information concerning any MHS device in his design.

ii) A second role is Customer Design : just like any subcontractor, upon customer request, MHS will develop specific applications so as to present a complete fully functional package to the customer.

iii) Another aspect of Customer Support is Advance Application, a more long-term support. This generates Aplication notes and Design ideas for future circuits and product improvement.

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Research and development

i) Hardware : develop emulators that guarantee full development support for new processors (specifically CMOS devices); develop board level products for complete CMOS systems.

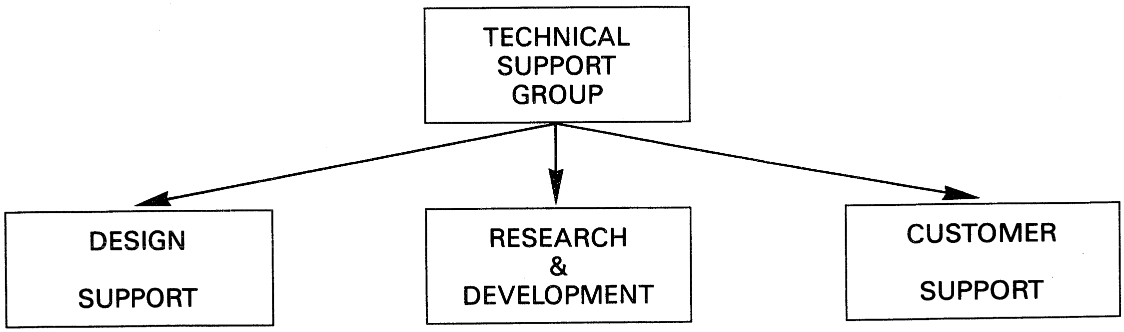
ii) Software : develop software for new microprocessor compatibility; develop new utility programs for increased development system efficiency. All software developed by MHS is available to the customer.

Design support

i) This function is internal to MHS and guarantees full support for the MHS design group when it comes to debugging and testing new devices. This also allows the engineers in the Support group to gain in-depth knowledge of the products produced by MHS, and therefore give even better support to the customer.

With this kind of support, MHS customers can depend on getting answers to all questions, solutions to most problems, whether hardware or software, and the knowledge needed to use MHS integrated circuits in the best way possible.

Matra-Harris Semiconducteurs Technical Support



DESIGN SUPPORT

- Prototype design
- New product test aid

RESEARCH & DEVELOPMENT

- Emulator design
- Board design
- Cross-assemblers
- Utility programs

CUSTOMER SUPPORT

- Customer aid
- Customer design
- Advanced application

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Telecommunication circuits 7

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Product Index

ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under ''Absolute Maximum Ratings'' may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect devices reliability. The conditions listed under ''Electrical Characteristics'' are the only conditions recommended for satisfactory operation.

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MHS

MATRA-HARRIS SEMICONDUCTEURS

data sheet

HC-5510/HC-5511
MONOLITHIC CODECs

PRELIMINARY

FEATURES

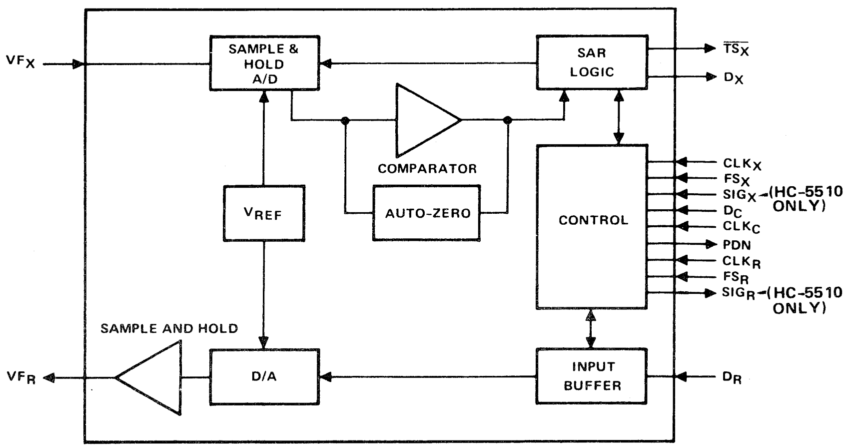
- LOW OPERATION POWER 45mW TYPICAL
- LOW STANDBY POWER 1mW TYPICAL
- ±5V OPERATION
- TTL COMPATIBLE DIGITAL INTERFACE
- TIME SLOT ASSIGNMENT OR ALTERNATE FIXED TIME SLOT MODES
- INTERNAL PRECISION REFERENCE
- INTERNAL SAMPLE AND HOLD CAPACITORS
- INTERNAL AUTO-ZERO CIRCUIT
- HC-5510 – μ-LAW CODING WITH SIGNALING CAPABILITIES
- HC-5511 – A-LAW CODING
- SYNCHRONOUS OR ASYNCHRONOUS OPERATION

DESCRIPTION

The HC-5510 and HC-5511 are monolithic PCM CODECs implemented with double-poly CMOS technology. The HC-5510 is intended for μ-law applications and contains logic for μ-law signaling insertion and extraction. The HC-5511 is intended for A-law applications.

Each device contains separate D/A and A/D circuitry, all necessary sample and hold capacitors, a precision voltage reference and internal auto-zero circuit. A serial control port allows an external controller to individually assign the PCM input and output ports to one of up to 32 time slots or to place the CODEC into a power-down mode. Alternately, the HC-5510/HC-5511 may be operated in a fixed time slot mode. Both devices are intended to be used with the HC-5512 monolithic PCM filter which provides the input anti-aliasing function for the encoder and smoothes the output of the decoder and corrects for the sin x/x distortion introduced by the decoder sample and hold output.

FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	-25°C to +125°C
Storage Temperature	-65°C to +150°C
V_{CC} with Respect to GNDD	7V
V_{CC} with Respect to V_{BB}	14V
V_{BB} with Respect to GNDD	-7V
Voltage at Any Input or Output	V_{BB} -0.3V to V_{CC} +0.3V
Lead Temperature (Soldering, 10 seconds)	300°C

DC ELECTRICAL CHARACTERISTICS

Unless otherwise noted, T_A = 0°C to 70°C, V_{CC} = 5.0V ±5%, V_{BB} = -5.0V ±5%. Typical characteristics are specified at V_{CC} = 5.0V and T_A = 25°C. All digital signals are referenced to GNDD. All analog signals are referenced to GNDA.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
DIGITAL INTERFACE						
I_I	Input Current	-10		10	μA	$0 < V_{IN} < V_{CC}$
V_{IL}	Input Low Voltage			0.6	V	
V_{IH}	Input High Voltage	2.2			V	
V_{OL}	Output Low Voltage			0.4 0.4 0.4 0.4	V V V V	D_X, I_{OL} = 4.0mA $\overline{SIG}_R$, I_{OL} = 0.5mA $\overline{TS}_X$, I_{OL} = 3.2mA, Open Drain PDN, I_{OL} = 1.6mA
V_{OH}	Output High Voltage	2.4 2.4			V V	D_X, I_{OH} = 6mA SIG_R, I_{OH} = 0.6mA
ANALOG INTERFACE						
Z_I	VF_X Input Impedance when Sampling	2.0			kΩ	Resistance in Series with Approximately 70pF
Z_O	Output Impedance at VF_R			10		$-3.1V < VF_R < 3.1V$
V_{OS}	Output Offset Voltage at VF_R	-25		25	mV	D_R = PCM Zero Code, HC-5510 or Alternating ±1 Code, HC-5511
I_{IN}	Analog Input Bias Current	-0.1		0.1	μA	V_{IN} = 0V
R1 x C1	DC Blocking Time Constant	4.0			ms	
C1	DC Blocking Capacitor	0.1			μF	
R1	Input Bias Resistor			50	kΩ	
POWER DISSIPATION						
I_{CC0}	Standby Current, V_{CC}		0.1	0.4	mA	
I_{BB0}	Standby Current, V_{BB}		0.0	0.1	mA	
I_{CC1}	Operating Current, V_{CC}		4.5	8.0	mA	
I_{BB1}	Operating Current, V_{BB}		4.5	8.0	mA	

SPECIFICATIONS (Continued)

AC ELECTRICAL CHARACTERISTICS Unless otherwise noted, the analog input is a 0dBm0, 1.02kHz sine wave. The digital input is a PCM bit stream generated by passing a 0dBm0, 1.02kHz sine wave through an ideal encoder. All output levels are sin x/x corrected.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
	Absolute Level					The nominal 0dBm0 levels for the HC-5510 and HC-5511 are 1.520 Vrms and 1.525 Vrms respectively. The resulting nominal overload level is 3.096V peak for both devices. All gain measurements for the encode and decode portions of the HC-5510/ HC-5511 are based on these nominal levels after the necessary sin x/x corrections are made.
G_{RA}	Receive Gain, Absolute	-0.1		0.1	dB	T = 25°C, V_{CC} =+5V, V_{BB} = -5V
G_{RAT}	Absolute Receive Gain Variation with Temperature	-0.05		0.05	dB	T = 0°C to 70°C
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	-0.07		0.07	dB	V_{CC} = 5V ±5%, V_{BB} =-5V±5%
G_{XA}	Transmit Gain, Absolute	-0.1		0.1	dB	T = 25°C, V_{CC} = 5V, V_{BB} = -5V
G_{XAT}	Absolute Transmit Gain Variation with Temperature	-0.05		0.05	dB	T = 0°C to 70°C
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	-0.07		0.07	dB	V_{CC} = 5V ±5%, V_{BB} = -5V ±5%
G_{RAL}	Absolute Receive Gain Variation with Level	-0.3 -0.2 -0.4 -1.0		0.3 0.2 0.4 1.0	dB dB dB dB	CCITT Method 2 Relative to -10dBm0 0dBm0 to 3dBm0 -40dBm0 to 0dBm0 -50dBm0 to -40dBm0 -55dBm0 to -50dBm0
G_{XAL}	Absolute Transmit Gain Variation with Level	-0.3 -0.2 -0.4 -1.0		0.3 0.2 0.4 1.0	dB dB dB dB	CCITT Method 2 Relative to -10dBm0 0dBm0 to 3dBm0 -40dBm0 to 0dBm0 -50dBm0 to -40dBm0 -55dBm0 to -50dBm0
S/D_R	Receive Signal to Distortion Ratio	35 29 25			dBc dBc dBc	Sinusoidal Test Method Input Level -30dBm0 to 0dBm0 -40dBm0 -45dBm0
S/D_X	Transmit Signal to Distortion Ratio	35 29 25			dBc dBc dBc	Sinusoidal Test Method Input Level -30dBm0 to 0dBm0 -40dBm0 -45dBm0
N_R	Receive Idle Channel Noise			0	dBnrc0	D_R = Steady State PCM Code
N_X	Transmit Idle Channel Noise			13 -67	dBrnc0 dBm0p	HC-5510, VF_X = 0V (no signalling) HC-5511, VF_X = 0V
HD_R	Receive Harmonic Distortion			-47	dB	2nd or 3rd Harmonic
HD_X	Transmit Harmonic Distortion			-47	dB	2nd or 3rd Harmonic
$PPSR_R$	Positive Power Supply Rejection, Receive	40			dB	D_R = Steady PCM Code, V_{CC} = $5.0V_{DC}$ +20mVrms, f = 1.02kHz
$PPSR_X$	Positive Power Supply Rejection, Transmit	50			dB	Input Level = 0V, V_{CC} = $5.0V_{DC}$ +20mVrms, f = 1.02kHz
$NPSR_R$	Negative Power Supply Rejection, Receive	45			dB	D_R = Steady PCM Code, V_{BB} = $-5.0V_{DC}$ +20mVrms, f = 1.02kHz
$NPSR_X$	Negative Power Supply Rejection Transmit	50			dB	Input Level = 0, V_{BB} = $-5.0V_{DC}$ +20mVrms, f = 1.02kHz
CT_{XR}	Transmit to Receive Crosstalk			-75	dB	D_R = Steady PCM Code
CT_{RX}	Receive to Transmit Crosstalk			-70	dB	Transmit Input Level = 0V

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SPECIFICATIONS (Continued)

TIMING SPECIFICATIONS

Unless otherwise noted, T_A = 0°C to 70°C, V_{CC} = 5.0 ±5%, V_{BB} = -5.0 ±5%. All digital signals are referenced to GNDD and measured at V_{IL} and V_{IH} levels as indicated in the timing waveforms.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
t_{PC}	Period of Clock	488			ns	CLK_C, CLK_R, CLK_X
t_{RC}, t_{FC}	Rise and Fall Time of Clock			30	ns	CLK_C, CLK_R, CLK_X
t_{WCH}	Width of Clock High	165			ns	CLK_C, CLK_R, CLK_X
t_{WCL}	Width of Clock Low	165			ns	CLK_C, CLK_R, CLK_X
$t_{A/D}$	A/D Conversion Time			16	Time Slots	From End of Encoder Time Slot to Completion of Conversion
$t_{D/A}$	D/A Conversion Time			2	Time Slots	From End of Decoder Time Slot to Transition of VF_R
t_{SDC}	Set-Up Time, D_C to CLK_C	100			ns	
t_{HDC}	Hold Time, CLK_C to D_C	100			ns	
t_{SFC}	Set-Up Time FS_X or CLK_X	100			ns	
t_{HFX}	Hold Time, CLK_X to FS_X	100			ns	
t_{DZX}	Delay Time to Enable D_X on TS Entry			125	ns	C_L = 150pF
t_{DDX}	Delay Time, CLK_X to D_X			125	ns	C_L = 150pF
t_{DXZ}	Delay Time, D_X to High Impedance State on TS Exit	50		165	ns	C_L = 0pF
t_{DTSL}	Delay to $\overline{TS}_X$ Low	30		185	ns	$0 \leq C_L \leq$ 150pF
t_{DTSH}	Delay to $\overline{TS}_X$ Off	30		185	ns	C_L = 0pF
t_{SSX}	Set-Up Time, SIG_X to CLK_X	100			ns	
t_{HSX}	Hold Time, CLK_X to SIG_X	100			ns	
t_{SFR}	Set-Up Time, FS_R to CLK_R	100			ns	
t_{HFR}	Hold Time, CLK_R to FS_R	100			ns	
t_{SDR}	Set-Up Time, D_R to CLK_R	40			ns	
t_{HDR}	Hold Time, CLK_R to D_R	30			ns	
t_{DSR}	Delay Time, CLK_R to SIG_R			300	ns	C_L = 100pF

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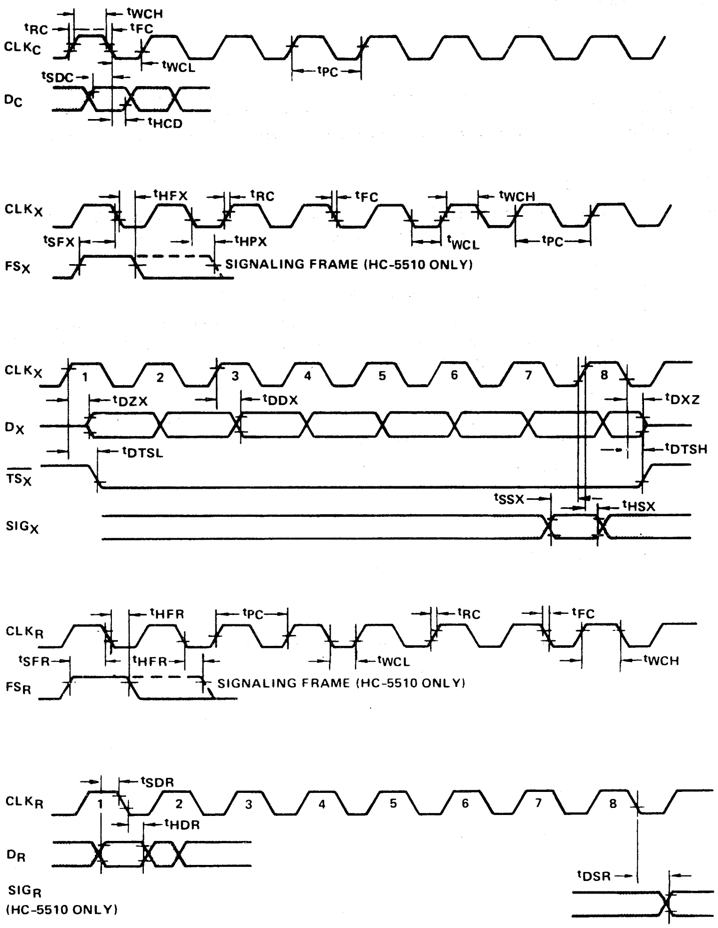
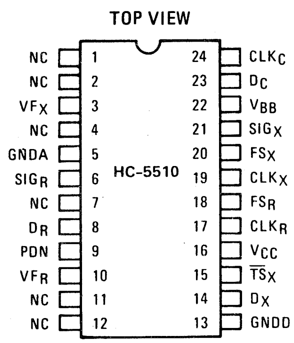
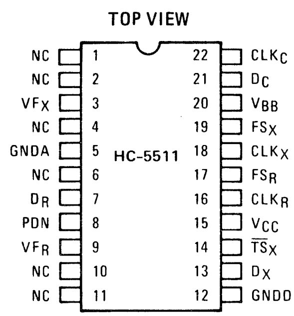
TIMING WAVEFORMS



PINOUTS





DESCRIPTION OF PIN FUNCTIONS

HC-5510

PIN NO.	SYMBOL	DESCRIPTION
1	NC	Unused
2	NC	Unused
3	VR_X	Analog input to the encoder. This signal will be sampled at the end of the encoder time slot and the resulting PCM code will be shifted out during the subsequent encode time slot.
4	NC	Unused
5	GNDA	Analog ground. All analog signals are referenced to this pin.
6	SIG_R	Receive signaling bit output. During receive signaling frames the least significant (last) bit shifted into D_R is internally latched and appears at this output-SIG_R will then remain valid until changed during a subsequent receive signaling frame or reset by a power-down command.
7	NC	Unused
8	D_R	Serial PCM data input to the decoder. During the decoder time slot, PCM data is shifted into D_R, most significant bit first, on the falling edge of CLK_R.
9	PDN	TTL output level which goes high when the CODEC is in the power-down mode. May be used to power-down other circuits associated with the PCM channel. Can be wire ANDed with other PDN outputs.
10	VF_R	Analog output from the decoder. The decoder sample and hold amplifier is updated approximately 15μs after the end of the decode time slot.
11	NC	Unused
12	NC	Unused
13	GNDD	Digital ground. All digital levels are referenced to this pin.
14	D_X	Serial PCM "Three-State" output from the encoder. During the encoder time slot, the PCM code for the previous sample of VF_X is shifted out, most significant bit first, on the rising edge of CLK_X.
15	$\overline{TS}_X$	Time slot output. This TTL compatible open-drain output pulses low during the encoder time slot. May be used to enable external "Three-State" bus drivers if highly capacitive loads must be driven. Can be wire ANDed with other $\overline{TS}_X$ outputs.
16	V_{CC}	5V (±5%) input.
17	CLK_R	Master decoder clock input used to shift in the PCM data on D_R and to operate the decoder sequencer. May operate at 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with CLK_X or CLK_C.
18	FS_R	Decoder frame sync pulse. Normally occurring at an 8kHz rate, this pulse is nominally one CLK_R cycle wide. Extending the width of FS_R to two or more cycles of CLK_R signifies a receive signaling frame.
19	CLK_X	Master encoder clock input used to shift out the PCM data on D_X and to operate the encoder sequencer. May operate at 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with CLK_R or CLK_C.
20	FS_X	Encoder frame sync pulse. Normally occurring at an 8kHz rate, this pulse is nominally one CLK_X cycle wide. Extending the width of FS_X to two or more cycles of CLK_X signifies a transmit signaling frame.
21	SIG_X	Transmit signaling input. During a transmit signaling frame, the signal at SIG_X is shifted out of D_X in place of the least significant (last) bit of PCM data.
22	V_{BB}	-5V (±5%) input.
23	D_C	Serial control data input. Serial data on D_C is shifted into the CODEC on the falling edge of CLK_C. In the fixed time slot mode, D_C doubles as a power-down input.
24	CLK_C	Control clock input used to shift serial control data into D_C. CLK_C must pulse 8 times during a period of time less than or equal to one frame time, although the 8 pulses may overlay a frame boundary. CLK_C need not be synchronous with CLK_X or CLK_R. Connecting CLK_C continuously high places the HC-5510/HC-5511 into the fixed time slot mode.

DESCRIPTION OF PIN FUNCTIONS (Continued)

HC-5511

PIN NO.	SYMBOL	DESCRIPTION
1	NC	Unused
2	NC	Unused
3	VF_X	Analog input to the encoder. This signal will be sampled at the end of the encoder time slot and the resulting PCM code will be shifted out during the subsequent encode time slot.
4	GNDA	Analog ground. All analog signals are referenced to this pin.
6	NC	Unused
7	D_R	Serial PCM data input to the decoder. During the decoder time slot, PCM data is shifted into DR, most significant bit first, on the falling edge of CLK_R.
8	PDN	Open drain output which turns off when the CODEC is in the power-down mode. May be used to power-down other circuits associated with the PCM channel. Can be wire ANDed with other PDN outputs.
9	VF_R	Analog output from the decoder. The decoder sample and hold amplifier is updated approximately 15μs after the end of the decode time slot.
10	NC	Unused
11	NC	Unused
12	GNDD	Digital ground. All digital levels are referenced to this pin.
13	D_X	Serial PCM "Three-State" output from the encoder. During the encoder time slot, the PCM code for the previous sample of VF_X is shifted out, most signficant bit first, on the rising edge of CLK_X.
14	$\overline{TS}_X$	Time slot output. This TTL compatible open-drain output pulses low during the encoder time slot. May be used to enable external "Three-State" bus drivers if highly capacitive loads must be driven. Can be wire ANDed with other $\overline{TS}_X$ outputs.
15	V_{CC}	5V (±5%) input.
16	CLK_R	Master decoder clock input used to shift in the PCM data on D_R and to operate the decoder sequencer. May operate at 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with CLK_X or CLK_C.
17	FS_R	Decoder frame sync pulse. Normally occurring at an 8kHz rate, this pulse is nominally one CLK_R cycle wide.
18	CLK_X	Master encoder clock input used to shift out the PCM data on D_X and to operate the encoder sequencer. May operate at 1.536MHz, 1.544MHz, or 2.048MHz. May be asynchronous with CLK_R or CLK_C.
19	FS_X	Encoder frame sync pulse. Normally occurring at an 8kHz rate, this pulse is nominally one CLK_X cycle wide.
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FUNCTIONAL DESCRIPTION

Power-Up

Upon application of power, internal circuitry initializes the CODEC and places it into the power-down mode. No sequencing of 5V or -5V is required. In the power-down mode, all non-essential circuits are deactivated, the Three-State PCM data output D_X is placed in the high impedance state and the receive signaling output of the HC-5510, SIG_R, is reset to logical zero. Once in the power-down mode, the method of activating the HC-5510/5511 depends on the chosen mode of operation, time slot assignment or fixed time slot.

Time Slot Assignment Mode

The time slot assignment mode of operation is selected by maintaining CLK_C in a normally low state. The state of the CODEC is updated by pulsing CLK_C eight times within a period of 125 μs or less. The falling edge of each clock pulse shifts the data on the D_C input into the CODEC. The first two control bits determine if the subsequential control bits B3-B8 are to specify the time slot for the encoder (B1 = 0), the decoder (B2 = 0) or both (B1 and B2 = 0) or if the CODEC is to be placed into the power-down mode (B1 and B2 = 1). The desired action will take place upon the occurrence of the second frame sync pulse following the first pulse of CLK_C. Assigning a time slot to either the encoder or decoder will automatically power-up the entire CODEC circuit. The D_X output and D_R input, however, will be inhibited for one additional frame to allow the analog circuitry time to stabilize. If separate time slots are to be assigned to the encoder and the decoder, the encoder time slot should be assigned first. This is necessary because up to four frames are required to assign both time slots separately, but only three frames are necessary to activate the D_X output. If the encode time slot has not been updated the PCM data will be outputed during the previously assigned time slot which may now be assigned to another CODEC.

Fixed Time Slot Mode

There are several ways in which the HC-5510/5511 may operate in the fixed time slot mode. The first and easiest method is to leave CLK_C disconnected or to connect CLK_C to V_{CC}. In this situation, D_C behaves as a power-down input. When D_C goes low, both encode and decode time slots are set to one on the second subsequent frame sync pulse. Time slot one corresponds to the eight CLK_X or CLK_R cycles starting one cycle from the nominal leading edge of FS_X or FS_R respectively. As in the time slot assignment mode, the D_X output is inhibited for one additional frame after the circuit is powered up. A logical "1" on D_C powers the CODEC down on the second subsequent FS_X pulse.

A second fixed time slot method is to operate CLK_C continuously. Placing a "1" on D_C will then cause the serial control register to fill up with ones. With B1 and B2 equal to "1" the CODEC will power-down. Placing a "0" on D_C will cause the serial control register to fill up with zeroes, assigning time slot one to both the encoder and decoder and powering up the device. One important restriction with this method of operation is that the rising transition of D_C must occur at least 8 cycles of CLK_C prior to FS_X. If this restriction is not followed, it is possible that on the frame prior to power-down, the encoder could be assigned to an incorrect time slot (e.g., 1, 3, 7, 15 or 31), resulting in a possible PCM bus conflict.

Serial Control Port

When the HC-5510/HC-5511 is operated in the time slot assignment mode or the fixed time slot mode with continuous clock, the data on D_C is shifted into the serial control register, bit 1 first. In the time slot assignment mode, depending on B1 and B2, the data in the RCV or XMT time slot registers is updated at the second FS_R or FS_X pulse after the first CLK_C pulse, or the CODEC is powered down. In the continuous clock fixed time slot mode, the CODEC is powered up or down at every second FS_R or FS_X pulse. The control register data is interpreted as follows:

B1	B2	ACTION
0	0	Assign Time Slot to Encoder and Decoder
0	1	Assign Time Slot to Encoder
1	0	Assign Time Slot to Decoder
1	1	Power-Down CODEC

B3	B4	B5	B6	B7	B8	TIME SLOT
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
0	0	0	0	1	1	4
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	1	1	1	0	63
1	1	1	1	1	1	64

During the power-down command, bits 3 through 8 are ignored. Note that with 64 possible time slot assignments it is frequently possible to assign a time slot which does not exist. This can be useful to disable an encoder or decoder without powering down the CODEC.

Signaling

The HC-5510 μ-law CODEC contains circuitry to insert and extract signaling information for the PCM data. The transmit signaling frame is signified by widening the FS_X pulse from one cycle of CLK_X to two or more cycles.

When this occurs, the data present on the SIG_X input at the eighth clock pulse of the encode time slot is inserted into the last bit of the PCM data stream. A receive signaling frame is indicated in a similar fashion by widening the FS_R pulse to two or more cycles of CLK_R.

During a receive signaling frame, the last PCM bit shifted in is latched into a flip-flop and appears at the SIG_R output. This output will remain unchanged until the next signaling frame, until a power-down is executed or until power is removed from the device. Since the least significant bit of the PCM data is lost during a signaling frame, the decoder interprets the bit as a "1/2" (i.e., half way between a "0" and a "1"). This minimizes the noise and distortion due to the signaling.

FUNCTIONAL DESCRIPTION (Continued)

Encoding Delay

The encoding process begins immediately at the end of the encode time slot and is concluded no later than 17 time slots later. In normal applications, this PCM data is not shifted out until the next time slot 125μs later, resulting in an encoding delay of 125μs. In some applications it is possible to operate the CODEC at a higher frame rate to reduce this delay. With a 2.048MHz clock, the FS rate could be increased to 15kHz reducing the delay from 125μs to 67μs.

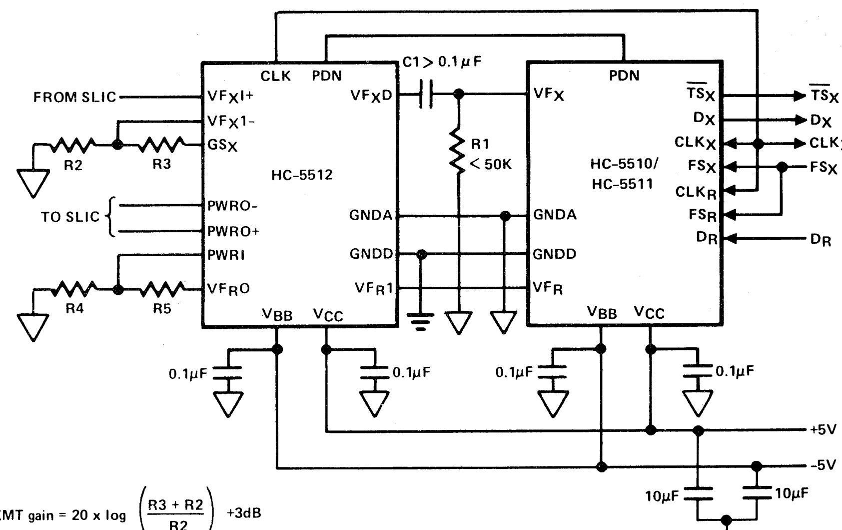
Decoding Delay

The decoding process begins immediately after the end of the decoder time slot. The output of the decoder sample and hold amplifier is updated 28 CLK_R cycles later. The decoding delay is therefore approximately 28 clock cycles plus one half of a frame time or 81μs for a 1.544MHz system with an 8kHz frame rate or 76μs for a 2.048MHz system with an 8kHz frame rate. Again, for some applications the frame rate could be increased to reduce this delay.

Typical Application

A typical application of the HC-5510/HC-5511 used in conjunction with the HC-5512 PCM filter is shown. The values of resistor R1 and D_C blocking capacitor C1, are noncritical. The capacitor value should exceed 0.1μF, R1 should be less than 50kΩ, and the product R1 x C1 should exceed 4ms.

TYPICAL APPLICATION



$$\text{XMT gain} = 20 \times \log\left(\frac{R3 + R2}{R2}\right) + 3\text{dB}$$

$$\text{RCV gain} = 20 \times \log\left(\frac{R4}{R4 + R5}\right)$$

The power supply decoupling capacitors should be 0.1μF. In order to take advantage of the excellent noise performance of the HC-5510/HC5511/HC-5512, care must be taken in board layout to prevent coupling of digital noise into the sensitive analog lines.

MHS MATRA-HARRIS SEMICONDUCTEURS

data sheet

HC-5512/5512 A
PCM MONOLITHIC FILTE

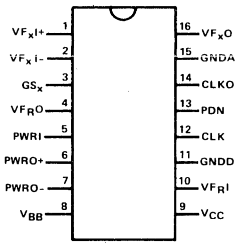
FEATURES

- EXCEEDS ALL D3/D4 AND CCITT SPECIFICATIONS
- +5V, -5V POWER SUPPLIES
- LOW POWER CONSUMPTION:
  45mW (600Ω 0dBm LOAD)
  30mW (POWER AMPS DISABLED)
- POWER DOWN MODE: 0.5mW
- 20dB GAIN ADJUST RANGE
- NO EXTERNAL ANTI-ALIASING COMPONENTS
- SIN x/x CORRECTION IN RECEIVE FILTER
- 50/60Hz REJECTION IN TRANSMIT FILTER
- TTL AND CMOS COMPATIBLE LOGIC
- ALL INPUT PROTECTED AGAINST STATIC DISCHARGE DUE TO HANDLING

PINOUT

DUAL-IN-LINE PACKAGE
TOP VIEW

Section 11 for Packaging



DESCRIPTION

The HC-5512/HC-5512A filter is a monolithic circuit containing both transmit and receive filters specifically designed for PCM CODEC filtering applications in 8kHz sampled systems.

The filter is manufactured using double-poly silicon gate CMOS technology. Switched capacitor integrators are used to simulate classical LC ladder filters which exhibit low component sensitivity.

TRANSMIT FILTER STAGE

The transmit filter is a fifth order elliptic low pass filter in series with a fourth order Chebyshev high pass filter. It provides a flat response in the passband and rejection of signals below 200Hz and above 3.4kHz.

RECEIVE FILTER STAGE

The receive filter is a fifth order elliptic low pass filter designed to reconstruct the voice signal from the decoded/demultiplexed signal which, as a result of the sampling process, is a stair-step signal having the inherent sin x/x frequency response. The receive filter approximates the function required to compensate for the degraded frequency response and restore the flat passband response.

FUNCTIONAL DIAGRAM

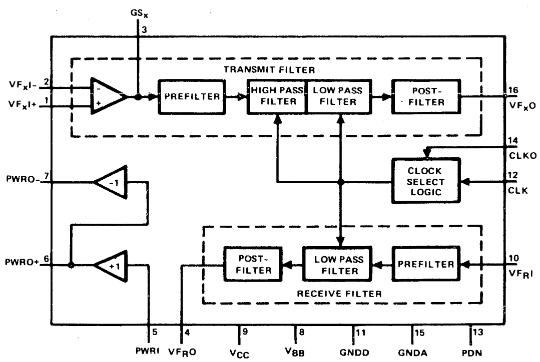


FIGURE 1

7

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	±7V
Power Dissipation	1W/Package
Input Voltage	±7V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	-25°C to +125°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC ELECTRICAL CHARACTERISTICS

Unless otherwise noted, T_A = 0°C to 70°C, V_{CC} = 5.0V±5%, V_{BB} = 5.0V±5%, clock frequency is 2.048 MHz. Typical parameters are specified at T_A = 25°C, V_{CC} = 5.0V, V_{BB} = -5.0V. Digital interface voltages measured with respect to digital ground, GNDD. Analog voltages measured with respect to analog ground, GNDA.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER DISSIPATION						
I_{CC0}	V_{CC} Standby Current	PDN = V_{DD}, Power Down Mode		50	100	μA
I_{BB0}	V_{BB} Standby Current	PDN = V_{DD}, Power Down Mode		50	100	μA
I_{CC1}	V_{CC} Operating Current	PWRI = V_{BB}, Power Amp Inactive		3.0	4.0	mA
I_{BB1}	V_{BB} Operating Current	PWRI = V_{BB}, Power Amp Inactive		3.0	4.0	mA
I_{CC2}	V_{CC} Operating Current	Note 1		4.6	6.4	mA
I_{BB2}	V_{BB} Operating Current	Note 1		4.6	6.4	mA
DIGITAL INTERFACE						
I_{INC}	Input Current, CLK	$V_{BB} \leq V_{IN} \leq V_{CC}$	−10		10	μA
I_{INP}	Input Current, PDN	$V_{BB} \leq V_{IN} \leq V_{CC}$	−100			μA
I_{INO}	Input Current, CLK0	$V_{BB} \leq V_{IN} \leq V_{CC} - 2V$	−10		−0.1	μA
V_{IL}	Input Low Voltage, CLK, PDN		0		0.8	V
V_{IH}	Input High Voltage, CLK, PDN		2.2		V_{CC}	V
V_{ILO}	Input Low Voltage, CLK0		V_{BB}		$V_{BB}+0.5$	V
V_{IIO}	Input Intermediate Voltage, CLK0		−0.8		0.8	V
V_{IHO}	Input High Voltage, CLK0		$V_{CC}-0.5$		V_{CC}	V
TRANSMIT INPUT OP AMP						
IB_xI	Input Leakage Current, VF_xI	$V_{BB} \leq VF_xI \leq V_{CC}$	−100		100	nA
RI_xI	Input Resistance, VF_xI	$V_{BB} \leq VF_xI \leq V_{CC}$	10			MΩ
VOS_xI	Input Offset Voltage, VF_xI	$-2.5V \leq V_{IN} \leq +2.5V$	−20		20	mV
V_{CM}	Common-Mode Range, VF_xI		-2.5		2.5	V
CMRR	Common-Mode Rejection Ratio	$-2.5V \leq V_{IN} \leq 2.5V$	60			dB
PSRR	Power Supply Rejection of V_{CC} or V_{BB}		60			dB
R_{OL}	Open Loop Output Resistance, GS_x			1		kΩ
R_L	Minimum Load Resistance, GS_x		10			kΩ
C_L	Maximum Load Capacitance, GS_x				25	pF
VO_xI	Output Voltage Swing, GS_x	$R_L \geq 10k$	±2.5			V
A_{VOL}	Open Loop Voltage Gain, GS_x	$R_L \geq 10k$	5,000			V/V
F_c	Open Loop Unity Gain Bandwidth, GS_x			2		MHz

SPECIFICATIONS

AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = 25°C. All parameters are specified for a signal level of 0 dBm0 at 1KHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRANSMIT FILTER (Transmit filter input op amp set to the non-inverting unity gain mode, with VF_xI = 1.1 Vrms unless otherwise noted.)						
RL_x	Minimum Load Resistance, VF_xO		10			kΩ
CL_x	Load Capacitance, VF_xO				25	pF
RO_x	Output Resistance, VF_xO			1	3	Ω
PSRR1	V_{CC} Power Supply Rejection, VF_xO	f = 1 kHz, VF_xI+ = 0 Vrms	30			dB
PSRR2	V_{BB} Power Supply Rejection, VF_xO	Same as Above	35			dB
GA_x	Absolute Gain	f = 1 kHz (HC-5512A) f = 1 kHz (HC-5512)	2.9 2.875	3.0 3.0	3.1 3.125	dB dB
GR_x	Gain Relative to GA_x	Below 50 Hz 50 Hz 60 Hz 200 Hz (HC-5512A) 200 Hz (HC-5512) 300 Hz to 3 kHz (HC-5512A) 300 Hz to 3 kHz (HC-5512) 3.3 kHz 3.4 kHz 4.0 kHz 4.6 kHz and Above	 −1.5 −1.5 −0.125 −0.15 −0.35 −0.70 	 −41 −35 −15 	−35 −35 −30 0 0.05 0.125 0.15 0.03 −0.1 −14 −32	dB dB dB dB dB dB dB dB dB dB dB
DA_x	Absolute Delay at 1 kHz				230	μs
DD_x	Differential Envelope Delay from 1 kHz to 2.6 kHz				60	μs
DP_x1	Single Frequency Distortion Products				−48	dB
DP_x2	Distortion at Maximum Signal Level	0.16 Vrms, 1 kHz Signal Applied to VF_xI+, Gain = 20 dB, R_L = 10k			−45	dB
NC_x1	Total C Message Noise at VF_xO			2	5	dBrnc0
NC_x2	Total C Message Noise at VF_xO	Gain Setting Op Amp at 20 dB, Non-Inverting, Note 3		3	6	dBrnc0
		T_A = 0°C to 70°C				
GA_xT	Temperature Coefficient of 1 kHz Gain			0.0004		dB/°C
GA_xS	Supply Voltage Coefficient of 1 kHz Gain	V_{CC} = 5.0V ± 5% V_{BB} = −5.0V ± 5%		0.01		dB/V
CT_{RX}	Crosstalk, Receive to Transmit $20 \log \frac{VF_xO}{VF_RO}$	Receive Filter Output = 2.2 Vrms VF_xI+ = 0 Vrms, f = 0.2 kHz to 3.4 kHz Measure VF_xO			−70	dB
GR_xL	Gaintracking Relative to GA_x	Output Level = +3 dBm0 +2 dBm0 to −40 dBm0 −40 dBm0 to −55 dBm0	−0.1 −0.05 −0.1		0.1 0.05 0.1	dB dB dB

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, $T_A = 25°C$. All parameters are specified for a signal level of 0 dBm0 at 1KHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVE FILTER (Unless otherwise noted, the receive filter is preceded by a sin x/x filter with an input signal level of 1.6 Vrms.)						
IB_R	Input Leakage Current, VF_RI	$-3.2V \le V_{IN} \le 3.2V$	−100		100	nA
RI_R	Input Resistance, VF_RI		10			MΩ
RO_R	Output Resistance, VF_RO			1	3	Ω
CL_R	Load Capacitance, VF_RO				25	pF
RL_R	Load Resistance, VF_RO		10			kΩ
PSRR3	Power Supply Rejection of V_{CC} or V_{BB}, VF_RO	VF_RI Connected to GNDA f = 1 kHz	35			dB
VOS_RO	Output DC Offset, VF_RO	VF_RI Connected to GNDA	−200		200	mV
GA_R	Absolute Gain	f = 1 kHz (HC-5512A) f = 1 kHz (HC-5512)	−0.1 −0.125	0 0	0.1 0.125	dB dB
GR_R	Gain Relative to Gain at 1 kHz	Below 300 Hz 300 Hz to 3.0 kHz (HC-5512A) 300 Hz to 3.0 kHz (HC-5512) 3.3 kHz 3.4 kHz 4.0 kHz 4.6 kHz and Above	 −0.125 −0.15 −0.35 −0.7 		0.125 0.125 0.15 0.03 −0.1 −14 −32	dB dB dB dB dB dB dB
DA_R	Absolute Delay at 1 kHz				100	μs
DD_R	Differential Envelope Delay 1 kHz to 2.6 kHz				100	μs
DP_R1	Single Frequency Distortion Products	f = 1 kHz			−48	dB
DP_R2	Distortion at Maximum Signal Level	2.2 Vrms Input to Sin x/x Filter, f = 1 kHz, R_L = 10k			−45	dB
NC_R	Total C-Message Noise at VF_RO			3	5	dBrnc0
GA_RT	Temperature Coefficient of 1 kHz Gain			0.0004		dB/°C
GA_RS	Supply Voltage Coefficient of 1 kHz Gain			0.01		dB/V
CT_{XR}	Crosstalk, Transmit to Receive $20 \log \frac{VF_RO}{VF_XO}$	Transmit Filter Output = 2.2 Vrms VF_RI = 0 Vrms, f = 0.3 kHz to 3.4 kHz Measure VF_RO			−70	dB
GR_RL	Gaintracking Relative to GA_R	Output Level = +3 dBm0 +2 dBm0 to −40 dBm0 −40 dBm0 to −55 dBm0 Note 5	−0.1 −0.05 −0.1		0.1 0.05 0.1	dB dB dB

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SPECIFICATIONS

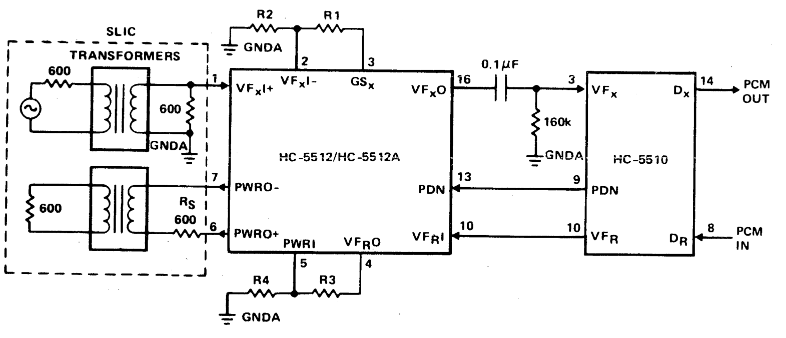
AC Electrical Characteristics (Continued)

Unless otherwise specified, $T_A = 25^oC$. All parameters are specified for a signal level of 0 dBm0 at 1kHz. The 0dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVE OUTPUT POWER AMPLIFIER						
IBP	Input Leakage Current, PWRI	$-3.2V \le V_{IN} \le 3.2V$	0.1		3	μA
RIP	Input Resistance, PWRI		10			MΩ
ROP1	Output Resistance, PWRO +, PWRO −	Amplifiers Active		1		Ω
CLP	Load Capacitance, PWRO +, PWRO −				500	pF
GA_P+	Gain, PWRI to PWRO +	$R_L = 600\Omega$ Connected Between PWRO + and PWRO −, Input Level = 0 dBm0 (Note 4)		1		V/V
GA_P-	Gain, PWRI to PWRO −			−1		V/V
GR_PL	Gaintracking Relative to 0 dBm0 Output Level	V = 2.05 Vrms, $R_L = 600\Omega$ (Notes 4, 5)	−0.1		0.1	dB
		V = 1.75 Vrms, $R_L = 300\Omega$ (Notes 4, 5)	−0.1		0.1	dB
S/D_P	Signal/Distortion	V = 2.05 Vrms, $R_L = 600\Omega$ (Notes 4, 5)			−45	dB
		V = 1.75 Vrms, $R_L = 300\Omega$ (Notes 4, 5)			−45	dB
VOSP	Output DC Offset, PWRO +, PWRO −	PWRI Connected to GNDA	−50		50	mV
PSRR5	Power Supply Rejection of V_{CC} or V_{BB}	PWRI Connected to GNDA	45			dB

Note 1: Maximum power consumption will depend on the load impedance connected to the power amplifier. The specification listed assumes 0 dBm is delivered to 600Ω connected from PWRO+ to PWRO−.
Note 2: Voltage input to receive filter at 0V VF_RO connected to PWRI, 600Ω from PWRO+ to PWRO−. Output measured from PWRO+ to PWRO−.
Note 3: The 0dBm0 level for the filter is assumed to be 1.54 Vrms measured at the output of the XMT or RCV filter.
Note 4: The odBm0 level for the power amplifiers is load dependent. For R_L = 600 to GNDA the 0dBm0 level is 1.43 Vrms measured at the amplifier output for R_L = 3000 the 0dBm0 level is 1.22Vrms.
Note 5: VF_RO connected to PWRI, input signal applied to VF_RI.

INTERFACE CIRCUIT FOR HC-5510 CODEC



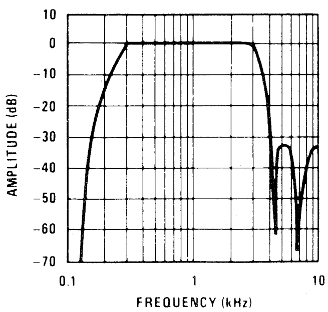
Note 1: Transmit voltage gain $\frac{R1 + R2}{R2} \times \sqrt{2}$ (The filter itself introduces a 3dB gain) (R1 + R2 ≥ 10k).
Note 2: Receive gain $\frac{R4}{R3 + R4}$
(R3 + R4 ≥ 10k)
Note 3: In the configuration shown, the receive filter power amplifiers will drive a 600Ω T to R termination to a signal level of 8.5dBm. An alternative arrangement, using a transformer winding ratio equivalent to 1.414:1 and 300Ω resistor, R_S, will provide a maximum signal level of 10.1dBm across a 600Ω termination impedance.

DESCRIPTION OF PIN FUNCTIONS

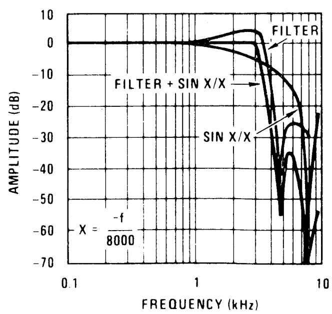
Pin No.	Name	Function
1	VF_xI+	The non-inverting input to the transmit filter stage.
2	VF_xI-	The inverting input to the transmit filter stage.
3	GS_x	The output used for gain adjustments of the transmit filter.
4	VF_RO	The low power receive filter output. This pin can directly drive the receive port of an electronic hybrid.
5	PWRI	The input to the receive filter differential power amplifier.
6	PWRO +	The non-inverting output of the receive filter power amplifier. This output can directly interface conventional transformer hybrids.
7	PWRO −	The inverting output of the receive filter power amplifier. This output can be used with PWRO + to differentially drive a transformer hybrid.
8	V_{BB}	The negative power supply pin. Recommended input is −5V.
9	V_{CC}	The positive power supply pin. The recommended input is 5V.
10	VF_RI	The input pin for the receive filter stage.
11	GNDD	Digital ground input pin. All digital signals are referenced to this pin.
12	CLK	Master input clock. Input frequency can be selected as 2.048 MHz, 1.544 MHz or 1.536 MHz.
13	PDN	The input pin used to power down the HC-5512 during idle periods. Logic 1 (V_{CC}) input voltage causes a power down condition. An internal pull-up is provided.
14	CLK0	This input pin selects internal counters in accordance with the CLK input clock frequency: **CLK** / **Connect CLK0 to:** 2048 kHz — V_{CC}; 1544 kHz — GNDD; 1536 kHz — V_{BB}. An internal pull-up is provided.
15	GNDA	Analog ground input pin. All analog signals are referenced to this pin. Not internally connected to GNDD.
16	VF_xO	The output of the transmit filter stage.

TYPICAL PERFORMANCE CHARACTERISTICS

Transmit Filter Stage



Receive Filter Stage



FUNCTIONAL DESCRIPTION

The HC-5512 monolithic filter contains four main sections; Transmit Filter, Receive Filter, Receive Filter Power Amplifier, and Frequency Divider/ Select Logic *(Figure 1)*. A brief description of the operation for each section is provided below.

Transmit Filter

The input stage of the transmit filter is a CMOS operational amplifier which provides an input resistance of greater than 10MΩ , a voltage gain of greater than 10,000, low power consumption (less than 3mW), high power supply rejection, and is capable of driving a 10kΩ load in parallel with up to 25pF. The inputs and output of the amplifier are accessible for added flexibility. Noninverting mode, inverting mode, or differential amplifier mode operation can be implemented with external resistors. It can also be connected to provide a gain of up to 20dB without degrading the overall filter performance.

The input stage is followed by a prefilter which is a two-pole RC active low pass filter designed to attenuate high frequency noise before the input signal enters the switched-capacitor high pass and low pass filters.

A high pass filter is provided to reject 200Hz or lower noise which may exist in the signal path. The low pass portion of the switched-capacitor filter provides stopband attenuation which exceeds the D3 and D4 specifications as well as the CCITT G712 recommendations.

The output stage of the transmit filter, the postfilter, is also a two-pole RC active low pass filter which attenuates clock frequency noise by at least 40dB. The output of the transmit filter is capable of driving a ±3.2V peak to peak signal into a 10kΩ load in parallel with up to 25pF.

Receive Filter

The input stage of the receive filter is a prefilter which is similar to the transmit prefilter. The prefilter attenuates high frequency noise that may be present on the receive input signal. A switched capacitor low pass filter follows the prefilter to provide the necessary passband flatness, stopband reejction and sin x/x gain correction. A postfilter which is similar to the transmit postfilter follows the low pass stage. It attenuates clock frequency noise and provides a low output impedance capable of directly driving an electronic subscriber-line-interface circuit.

Receive Filter Power Amplifiers

Two power amplifiers are also provided to interface to transformer coupled line circuits. These two amplifiers are driven by the output of the receive postfilter through gain settling resistors, R3, R4 *(Figure 2)*. The power amplifiers can be deactivated, when not required, by connecting the power amplifier input (pin 5) to the negative power supply V_{BB}. This reduces the total filter power consumption by approximately 10mW-20mW depending on output signal amplitude.

Power Down Control

A power down mode is also provided. A logic 1 power down command applied on the PDN pin (pin 13) will reduce the total filter power consumption to less than 1mW and clamp the power amplifier output to V_{BB}. Connect PDN to GNDD for normal operation.

Frequency Divider and Select Logic Circuit

This circuit divides the external clock frequency down to the switching frequency of the low pass and high pass switched capacitor filters. The divider also contains a TTL-CMOS interface circuit which converts the external TTL clock level to the CMOS logic level required for the divider logic. This interface circuit can also be directly driven by CMOS logic. A frequency select circuit is provided to allow the filter to operate with 2.048MHz, 1.544MHz or 1.536MHz clock frequencies. By connecting the frequency select pin CLKO (pin 14) to V_{CC}, a 2.048MHz clock input frequency is selected. Digital ground selects 1.544MHz and V_{BB} selects 1.536MHz.

APPLICATIONS INFORMATION

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Gain Adjust

Figure 2 shows the signal path interconnections between the HC-5512 and HC-5510 single channel CODEC. The transmit RC coupling components have been chosen both for minimum passband droop and to present the correct impedance to the CODEC during sampling.

Optimum noise and distortion performance will be obtained for the HC-5512/HC-5512A filter when operated with system peak overload voltages of ±2.5V to ±3.2V at VF_XO and VF_RO. When interfacing to a PCM CODEC with a peak overload voltage outside this range, further gain or attenuation may be required.

For example, the HC-5512 filter can be used with the HC-5510/5511 series CODEC which has a 5.5V peak overload voltage. A gain stage following the transmit filter output and an attenuation stage following the CODEC output are required.

Board Layout

Care must be taken in PCB layout to minimize power supply and ground noise. Analog ground (GNDA) of each filter should be connected to digital ground (GNDD) at a single point, which should be bypassed to both power supplies. Further power supply decoupling adjacent to each filter and CODEC is recommended. Ground loops should be avoided, both between GNDA and GNDD and between the GNDA traces of adjacent filters and CODECs.

HC-5541 A
PULSE/TONE DIALER

ADVANCE INFORMATION

■ Features

- GENERATES EITHER DTMF TONES OR DIAL PULSES
- INTERFACES WITH STANDARD KEYPADS (FORM A CONTACT OR 2 OF 8) OR 4 BIT CMOS µP BUS.
- 24 DIGIT LAST NUMBER REDIAL BOTH MODES
- USES INEXPENSIVE 3.5795 MHz TV COLOR BURST CRYSTAL
- REGULATED TONE OUTPUT AMPLITUDES
- 2.7 V to 6 V OPERATION
- TONE FREQUENCIES WITHIN 1 %
- SINGLE TONE CAPABILITY
- MEETS INTERNATIONAL STANDARDS FOR TONE LEVELS AND DISTORTION
- AUTOMATIC RECEIVER MUTE OUTPUT DURING SIGNALING
- MUTE, PAUSE, FLASHING AND CANCEL SPECIAL FUNCTIONS

Description

The HC-5541 A is a CMOS monolithic integrated circuit telephone dialer designed for applications where it is needed to produce either dial pulses or dial tones at will.

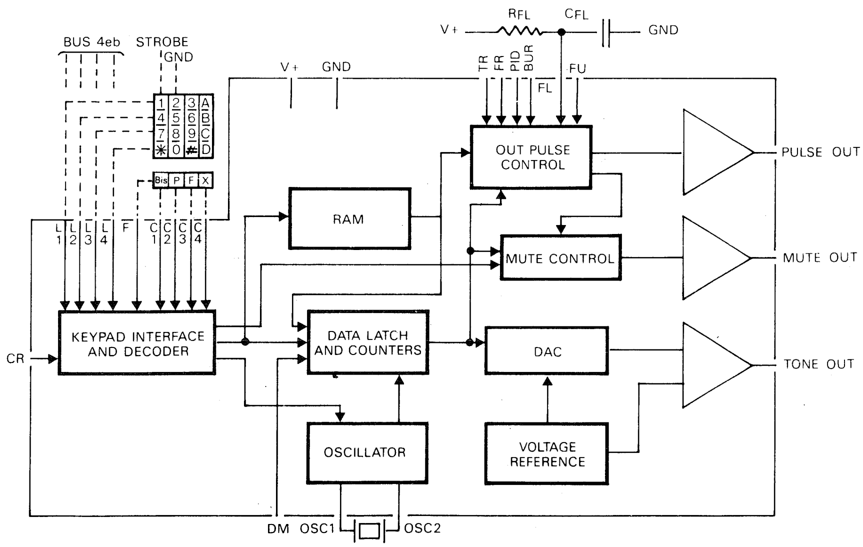
OUTPUTS

The HC-5541 A outputs dial pulses or dial tones on separate pins. Sixteen standard DTMF frequency pairs are provided, accurate to ± 1 %. For pulse outputs, the make/break ratio can be selected with a single pin to conform to either US or European standards. A mute output is provided to mute the receiver while output signals are being generated.

INPUTS

Data can be entered from a 4 × 4 keypad or a 4 bit microprocessor bus. In addition, the circuit can be driven from a standard 3×4 keypad plus one additional switch to select tones or pulses. Selection of keypad or microprocessor entry is controlled from a single pin.

Functional Diagram



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HC 5552/HC 5553
HC 5554/HC 5557

data sheet

MONOLITHIC CMOS Serial Interfac[e] CODEC/FILTER FAMILY

PRELIMINARY

Features

COMPLETE CODEC/FILTER (COMBO) Family

- HC 5552 - μ-LAW WITH SHORT FRAME SIGNALING (18 PIN)
- HC 5553 - μ-LAW WITH BOTH SHORT AND LONG FRAME SIGNALING (20 PIN)
- HC 5554 - μ-LAW WITHOUT SIGNALING (16 PIN)
- HC 5557 - A-LAW (16 PIN)
- LOW OPERATION POWER
- LOW STANDBY POWER
- + 5 / − 5 OPERATION
- MEETS OR EXCEED ALL D3/D4 AND CCITT SPECIFICATIONS
- TTL COMPATIBLE DIGITAL INTERFACES
- PCM DATA SERIAL INPUT/OUTPUT
- SYNCHRONOUS OR ASYNCHRONOUS OPERATION

Description

The MHS CODEC/FILTER (COMBO) Family includes A-Law and μ-Law monolithic CODEC/FILTER implemented with double-poly CMOS technology.

The transmit side of the device consists of an
- amplifier with external gain adjust
- RC active prefilter to eliminate high frequency noise
- switch capacitor band Pass Filter including a notch filter at 55 Hz to reject signals below 200 Hz and above 3400 Hz
- charge redistribution coder which samples and encodes filtered signal in the companded μ-Law or A-Law PCM format
- Precision voltage reference
- internal auto-zero network to cancel the transmit offset

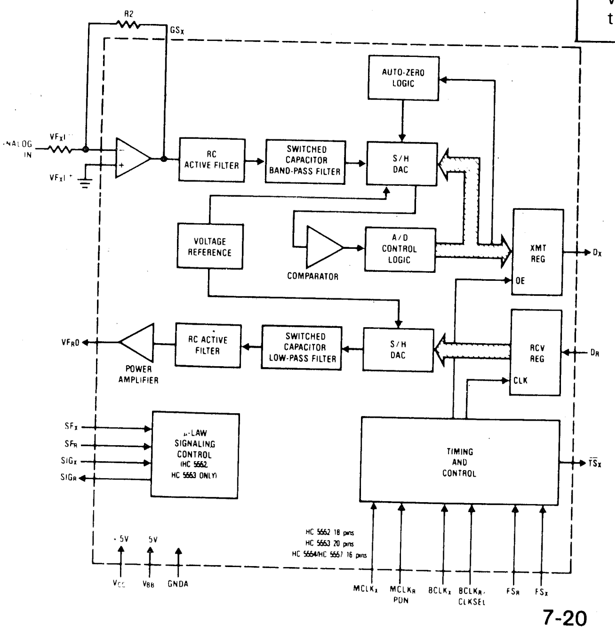
The receive side of the device consists of an
- expanding decoder (A-Law or μ-Law) to reconstruct the analog signal
- switch capacitor low pass filter which corrects for the sinx/x response of the decoder output and rejects signals above 3400 Hz
- RC active filter followed by a single ended power amplifier able to driver 600 OHM load

The PCM word is transmitted/received in serial compatible industry standard formats.

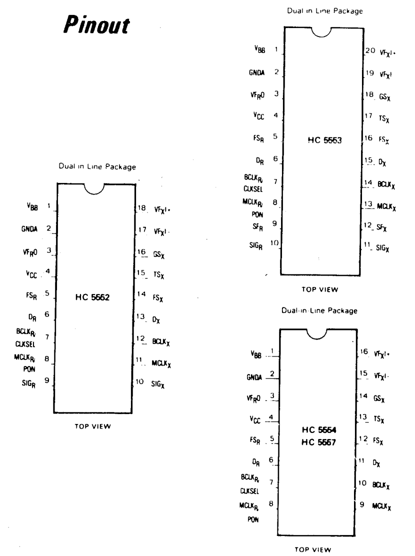
The device is operated with two (transmit and receive) master clocks (1.536 MHz, 1.544 MHz or 2.048 MHz) which may be asynchronous.

Also required are transmit and receive bit clocks which may vary from 64 KHz to 2.048 MHz and transmit and receive frame sync pulses.

Functional Diagram



Pinout



Electrical Specifications

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GNDD or GNDA	7V
V_{BB} to GNDD or GNDA	−7V
Voltage at any input	V_{CC} + 0.3V to V_{BB} − 0.3V
Voltage at any Digital Output	V_{CC} + 0.3V to GNDA − 0.3V
Voltage at any Analog Output	V_{CC} + 0.3V to V_{BB} − 0.3V
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	− 65°C to 150°C
Lead Temperature (Soldering 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted : V_{CC} = 5.0V ± 5 %, V_{BB} = 5V ± 5 %, GNDA = 0V.
T_A = 0°C to 70°C : typical characteristics specified at V_{CC} = 5.0V, V_{BB} = − 5.0V, T_A = 25°C ; all signals are referenced to GNDA

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INTERFACE						
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.2			V
V_{OL}	Output Low Voltage	D_X, I_L = 5.0mA SIG_R, I_L = 1.0mA			0.4 0.4	V V
V_{OH}	Output High Voltage	D_X, I_L = − 5.0mA SIG_R, I_L = − 1.0mA	2.4 2.4			V V
I_{IL}	Input Low Current	GNDA $\leqslant V_{IN} \leqslant V_{IL}$, All Digital Inputs	− 10		10	μA
I_{IH}	Input High Current	$V_{IH} \leqslant V_{IN} \leqslant V_{CC}$	− 10		10	μA
I_{OZ}	Output Current in High Impedance State (TRI-STATE)	D_X, GNDA $\leqslant V_O \leqslant V_{CC}$	− 50		50	μA
ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (ALL DEVICES)						
I_IXA	Input Leakage Current	− 2.5V $\leqslant$ V $\leqslant$ + 2.5V.VF_X + or VF_X−	− 1.0		1.0	μA
R_IXA	Input Resistance	− 2.5V $\leqslant$ V $\leqslant$ + 2.5V.VF_X + or VF_X −	10			MΩ
R_OXA	Output Resistance	Close Loop		1		Ω
R_LXA	Load Resistance	GS_X	10			kΩ
C_LXA	Load Capacitance	GS_X			50	pF
V_OXA	Output Level	GS_X.R_L = 10k	± 2.5	± 4.2		V
A_VXA	Voltage Gain	VF_X + to GS_X	5000			V/V
F_UXA	Unity Gain Bandwidth		1	2		MHz
$V_{OS}XA$	Offset Voltage		− 20	1	20	mV
$V_{CM}XA$	Common-Mode Voltage		− 3.5		+ 3.5	V
CMRRXA	Common-Mode Rejection Ratio		60	80		dB
PSRRXA	Power Supply Rejection Ratio		60	70		dB
ANALOG INTERFACE WITH RECEIVE FILTER (ALL DEVICES)						
R_ORF	Output Resistance	Pin VF_RO		1		Ω
R_LRF	Load Resistance	VF_RO = ± 2.5V	600			Ω
C_LRF	Load Capacitance				500	pF
POWER DISSIPATION (ALL DEVICES)						
PW0	When Power Down			2	10	mW
PW1	When Power Up			60	100	mW

Timing Specifications

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1/TPM	Frequency of master Clock	Depends on the Device Used and the $BCKL_R$/CLKSEL pin		1.536 1.544 2.048		MHz MHz
T_{WMH}	Width of Master Clock High		160			ns
T_{WML}	Width of Master Clock Low		160			ns
T_{RM}	Rise Time of Master Clock				50	ns
T_{FM}	Fall Time of Master Clock				50	ns
T_{HMB}	Holding Time from Master Clock to Bit Clock	Transmit side and Receive side in synchronous mode	0		50	ns
T_{PB}	Period of Bit Clock		0.488		15.625	μs
T_{WBH}	Width of Bit Clock High	V_{IH} = 2.4V	160			ns
T_{WBL}	Width of Bit Clock Low	V_{IL} = 0.6V	160			ns
T_{RB}	Rise Time of Bit Clock	t_{PB} = 488 ns			50	ns
T_{FB}	Fall Time of Bit Clock	t_{PB} = 488 ns			50	ns
T_{HBF}	Holding Time from Bit Clock Low to Frame Sync	Long Frame Only	0			ns
T_{HOLD}	Holding Time from Bit Clock High to Frame Sync	Short Frame Only	0			ns
T_{SFB}	Set-Up Time from Frame Sync to Bit Clock High	Long Frame Only (Note 1)	50			ns
T_{DBD}	Delay Time from $BCLK_X$ High to Data Valid	Load = 150 pF plus 2 LSTTL Loads	50		140	ns
T_{DFDZ}	Delay Time from $BCLK_X$ Low to Data Output Disabled	C_L = 0 pF to 150 pF Loads 8^{th}BCLKX trailing edge	0		165	ns
T_{HBSF}	Hold Time from $BCLK_{X/R}$ Low to Signal Frame Sync rising	5553 Only	0			ns
T_{SSFB}	Set-Up Time from Signal Frame Sync High to $BCLK_{X/R}$ rising	5553 Only	50			ns
T_{SSGB}	Set-Up Time from $SIG_X$to $BCLK_X$ rising	5552 and 5553	100			ns
T_{HBSG}	Hold Time from $BCLK_X$ High to SIG_X	5552 and 5553	50			ns
T_{SDB}	Set-Up Time from D_R Valid to $BCLK_{R/X}$ Low		50			ns
T_{HBD}	Hold Time from $BCLK_{R/X}$ Low to D_R Invalid		50			ns
T_{DFSSG}	Delay Time from $BCLK_R$ Low to SIG_R Valid	C_L = 50 pF.2 LSTTL Loads			300	ns
T_{HBSI}	Hold Time from 3rd period of $BCLK_{X/R}$ Low to Signaling Frame Sync falling	5553 Only	0			ns
TSF	Set-Up Time from $FS_{X/R}$ to $BCLK_{X/R}$ Low	Short Frame Sync Pulse (1 or 2 Bit Clock Periods Long) (Note 2)	100			ns

Timing Specifications (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
T_{HF}	Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$	Short Frame Sync Pulse (1 or 2 Bit Clock Periods Long) (Note 2)	100			ns
T_{HBFI}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS_X or FS_R) falling	Long Frame Sync Pulse (from 3 to 8 Bit Clock Periods Long)	0			ns
T_{WFL}	Minimum Width of the Frame Sync Pulse (Low Level)	64k Bit/s Operating Mode	1000		7500	ns
TDFDE	Delay Time from FS_X to data output enable	Long Frame	0		140	ns
TDBDE	Delay Time from $BCLK_X$ to data output enable	Short Frame	0		140	ns
$TSFB_{64kHz}$	Hold Time from $FS_{X/R}$ High to $BCLK_{X/R}$ Rising		300			ns
$THBFI_{64kHz}$	Hold Time from 8th Period of $BCLK_{X/R}$ Low to $FS_{X/R}$ Trailing Edge		50			ns
TDXP	Delay Time from $BCLK_X$ High to $\overline{TS_X}$ Low	Short Frame			140	ns
TDXP	Delay Time from FSX High to $\overline{TS_X}$ Low	Long Frame			140	ns
TDZC	Delay Time from $BCLK_X$ Low to $\overline{TS_X}$		0		165	ns

Note 1: For long frame sync timing FS_X and FS_R must go high or low while their respective bit clocks are low.

Note 2: For short frame sync timing FS_X and FS_R must go high while their respective bit clocks are high.

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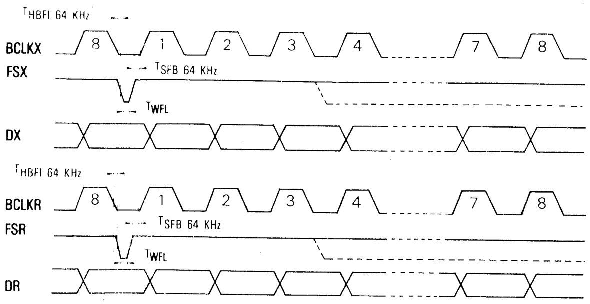
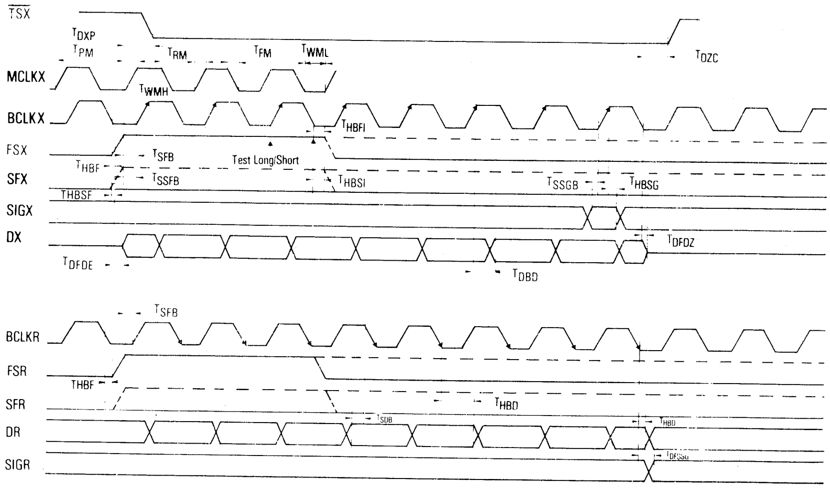
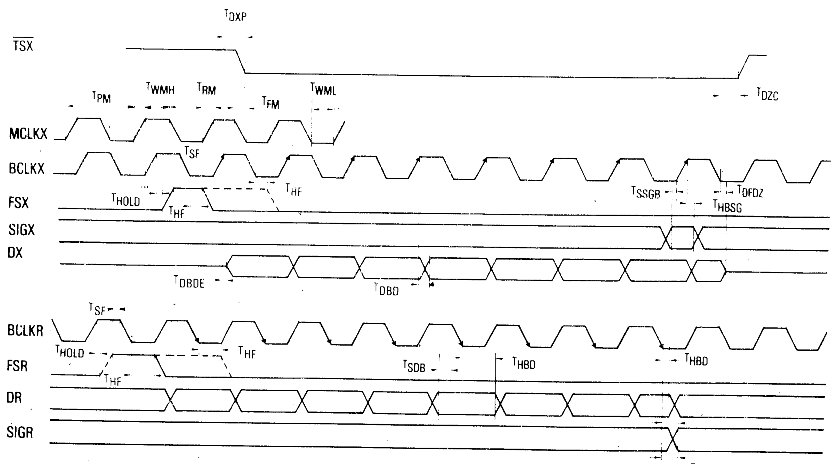


64 KBIT TIMING DIAGRAM



LONG FRAME SYNC TIMING



SHORT FRAME SYNC TIMING

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Transmission Characteristics (All Devices)

Unless otherwise specified : T_A = 0°C to 70°C, V_{CC} = 5V ± 5 %, V_{BB} = – 5V ± 5 %, GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity-GAIN non-inverting.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
AMPLITUDE RESPONSE						
	Absolute Levels	Nominal 0 dBm0 Level is 4 dBm (600Ω) 0 dBm0 5552 5553 5554 5557		 1.2277 1.2277		 Vrms Vrms
t_{MAX}		Max Overload Level		2.501 2.492		V_{DC} V_{DC}
G_{XA}	Transmit Gain, Absolute	T_A = 25°C, V_{CC} = 5V V_{BB} = – 5V, f = 1.02 Khz	– 0.15		0.15	dB
G_{XR}	Transmit Gain Relative to G_{XA}	f = 16 Hz f = 50 Hz f = 66 Hz f = 180 Hz f = 200 Hz f = 300 Hz – 3000 Hz f = 3400 Hz f = 3600 Hz f = 4000 Hz f = 4600 Hz and Up	 – 2.8 – 1.8 – 0.15 –0.7		– 40 – 40 – 40 – 0.2 – 0.125 + 0.15 + 0.125 0 – 14 – 32	dB dB dB dB dB dB dB dB dB dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	T_A = 0°C to 80°C			± 0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	V_{CC} = 5V ± 5 %, V_{BB} = – 5V ± 5 %			± 0.05	dB
G_{XRL}	Transmit Gain Variations with level	Sinusoidal Test Method Reference Level = – 10 dBm0 VF_XI + = – 40 dBm0 to + 3 dBm0 VF_XI + = – 50 dBm0 to – 40 dBm0 VF_XI + = – 55 dBm0 to – 50 dBm0	 – 0.2 – 0.5 – 1.6		 0.2 0.5 1.6	 dB dB dB
G_{RA}	Receive Gain, Absolute	f = 1.02 kHz	– 0.15		0.15	dB
G_{RR}	Receive Gain Relative to G_{RA}	f = 0 Hz to 3000 Hz f = 3400 Hz f = 3600 Hz f = 4000 Hz	– 0.15 – 0.7		+0.15 0.125 0 – 14	dB dB dB dB
G_{RAT}	Absolute receive Gain Variation with Temp.	T_A = 0°C to 80°C			± 0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	V_{CC} = 5V ± 5 %, V_{BB} = 5V ± 5 %			+ 0.05	dB
G_{RRL}	Receive Gain Variations with Level	Sinusoidal Test Method : Reference Input PCM Code Corresponds to an Ideally Encoded – 10 dBm0 Signal PCM Level = – 40 dBm0 to + 3 dBm0 PCM Level = – 50 dBm0 to – 40 dBm0 PCM Level = – 55 dBm0 to – 50 dBm0	 – 0.2 – 0.5 – 1.6		 + 0.2 + 0.5 + 1.6	 dB dB dB
VFRO	Receive Output Drive Level	R_L = 600Ω	– 2.5		2.5	V

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Transmission Characteristics (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ENVELOPE DELAY DISTORTION WITH FREQUENCY						
D_{XA}	Transmit Delay, Absolute	f = 1600 Hz		290	315	μs
D_{XR}	Transmit Delay, Relative to D_{XA}	f = 500 Hz – 600 Hz f = 600 Hz – 800 Hz f = 800 Hz – 1000 Hz f = 1000 Hz – 1600 Hz f = 1600 Hz – 2600 Hz f = 2600 Hz – 2800 Hz f = 2800 Hz – 3000 Hz		140 100 50 20 60 80 140	220 145 75 40 75 105 155	μs μs μs μs μs μs μs
D_{RA}	Receive Delay, Absolute	f = 1600 Hz		140	180	μs
D_{RR}	Receive Delay, Relative to D_{RA}	f = 500 Hz – 1600 Hz f = 1600 Hz – 2600 Hz f = 2600 Hz – 2800 Hz f = 2800 Hz – 3000 Hz		40 90 120 140	60 120 140 175	μs μs μs μs
NOISE						
NIX	Idle transmit noise (P message weighted)	600 load tied to the input			– 66	dBm0p
NIR	Idle receive noise (P message weighted)	PCM code equals zero			– 77	dBm0p
NRS	Noise single frequency	Receive input, connect to transmit output			– 53	dBm0
SIS	Spurious inband signal	f = 1020 Hz 0dBm0 transmit f = 1020 Hz 0dBm0 receive			– 46	dBm0
POWER SUPPLY REJECTION						
PSRX	Transmit power supply rejection	f = 0 Hz – 4000 Hz f = 4 KHz – 25 KHz f = 25 KHz – 50 KHz 100 mv RMS either supply	+ 40 + 40 + 36			dBp dB dB
PSRR	Receive power supply rejection	f = 0 Hz – 4000 Hz f = 4 KHz – 25 KHz f = 25 KHz – 50 KHz 100 mv RMS either supply	+ 40 + 40 + 36			dBp db dB
DISTORTION						
IMD	Inter-modulation distortion	Loop around measurement VF_X + = – 4 dBm0 to – 21 dBm0 2 frequencies in the range 300 Hz to 3400 hz			– 41	dB
CROSSTALK						
CTXR	Transmit to Receive Crosstalk 0dBm0 Transmit Level	f = 300 Hz – 3400 Hz DR = Steady PCM code			– 70	dB
CTRX	Receive to Transmit Crosstalk 0dBm0 receive Level	f = 300 Hz – 3400 Hz VFxt = 0V			– 70	dB

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Pin Description

5552 PIN NO	5553 PIN NO	5554 5557 PIN NO	NAME	FUNCTION
1	1	1	VBB	NEGATIVE POWER SUPPLY − 5V +/− 5 %
2	2	2	GNDA	ANALOG GROUND
3	3	3	VFRO	ANALOG OUTPUT OF THE RECEIVE FILTER
4	4	4	VCC	POSITIVE POWER SUPPLY 5V +/− 5 %
5	5	5	FSR	RECEIVE FRAME SYNC PULSE.AN 8 KHZ PULSE TRAIN WHICH ENABLES THE PCM WORD TO BE SHIFTED INTO THE RECEIVE REGISTER
6	6	6	DR	RECEIVE DATA INPUT. THE RECEIVE REGISTER CLOCKS IN DR INPUT WITH BIT CLOCK FALLING EDGE FOLLOWING AN FSR RISING EDGE
7	7	7	BCLKR & CLKSEL	BIT CLOCK WHICH SHIFTS DR INPUT INTO THE RECEIVE REGISTER. MAY VARY FROM 64 KHZ TO 2.048 MHZ. ALTERNATIVELY MAY BE A CLOCK SELECTION. SEE TABLE IN FUNCTIONAL DESCRIPTION FOR SYNCHRONOUS OPERATION
8	8	8	MCLKR PDN	RECEIVE MASTER CLOCK MUST BE 1.536 OR 1.544 OR 2.084 MHZ MAY BE ASYNCHRONOUS WITH BCLKR. IF MCLKR IS LOW, THE COMBO OPERATES IN SYNCHRONOUS MODE. IF MCLKR IS TIED HIGH, THE COMBO IS POWERED DOWN.
	9		SFR	WHEN HIGH DURING FSR, SFR INDICATES A RECEIVE SIGNALING FRAME
9	10		SIGR	THE SIGNALING BIT APPEARS AT THIS OUTPUT AFTER EACH RECEIVE SIGNALING FRAME
10	11		SIGX	SIGNALING DATA INPUT. THIS INPUT IS INSERTED IN PLACE OF LSB OF PCM WORD DURING SIGNALING FRAME
	12		SFX	WHEN HIGH DURING FSX, THIS INPUT INDICATES A LONG FRAME SIGNALING
11	13	9	MCLKX	TRANSMIT MASTER CLOCK.MUST BE 1.536 1.544 0R 2.048 MHz. MAY BE ASYNCHRONOUS WITH MCLKR
12	14	10	BCLKX	BIT CLOCK. MAY VARY FROM 64 KHZ TO 2.048 MHz, BUT MUST BE SYNCHRONOUS WITH MCLKX
13	15	11	DX	TRI-STATE PCM DATA OUTPUT
14	16	12	FSX	TRANSMIT FRAME SYNC PULSE. AN 8 KHz PULSE TRAIN WHICH ENABLES THE PCM WORD TO BE SHIFTED OUT THROUGH DX WITH BCLKX
15	17	13	$\overline{\text{TSX}}$	OPEN DRAIN OUTPUT PULL DOWN DURING TIME SLOT
16	18	14	GSX	ANALOG OUTPUT OF TRANSMIT AMPLIFIER USED TO SET THE GAIN
17	19	15	VFXI −	INVERTING INPUT OF TRANSMIT AMPLIFIER
18	20	16	VFXI +	NON INVERTING INPUT OF TRANSMIT AMPLIFIER

Functional Description

POWER UP/POWER DOWN

When the power supply is applied the combo is initialised in the power down mode. All the analog blocks are desactivated, Dx and VFRO are in their high impedance state. With a low level or a clock applied on MCLKR, the combo powers up, but will ignore the first FSX and FSR rising edges.

SYNCHRONOUS OPERATION

If no clock is applied to MCLKR the combo assumes a synchronous mode. MCLKX and BLCKX are used for both transmit and receive. In this mode BCLKR is used as a clock select. A high level or open circuit select the normal frequency, a low level selects the alternate frequency (see table below).

BCLKR/CLKSEL	5557	5552/5553
CLOCK	2.048 MHZ	1.544/1.536 MHZ
LOW	1.536/1.544 MHZ	2.048 MHZ
HIGH OR OPEN	2.048 MHZ	1.536/1.544 MHZ

ASYNCHRONOUS OPERATION

MCLKR is supplied separately from MCLKX and must be 2.048 MHZ for 5557 (a law) and 1.544 or 1.536 MHZ for 5552 5553 5554 (u law). BCLKX and BCLKR may operate from 64 KHZ to 2.048 MHZ. BCLKX must be synchronous with MCLKX but BCLKR may be asynchronous with MCLKR. FSX and FSR must be synchronous with their respective bit clock.

SHORT FRAME OPERATION

In the short frame operation FSX and FSR must be one bit clock period long. With FSX high during a falling edge of BCLKX the next rising edge of BCKLX enables the DX buffer to shift the sign bit out. The other bits are clocked out with the 7 following rising edges of BCLKX. The falling edge of the 8TH BCLKX pulse disables the DX buffer. With FSR high during a falling edge of BCLKR (BCLKX synchronous mode), the next 8 BCLKR (resp. BCLKX) falling edges latch the PCM word in the receive register, sign bit first. In short frame mode, FSX and FSR must go high during BCLKX and BCLKR high.

LONG FRAME OPERATION

In the long frame operation, FSX and FSR must be 3 bit clock periods or more (see timing). The DX buffer is directly enabled by FSX rising edge and the following rising edge of BCLKX shifts out the sign bit. The following 7 BCLKX rising edges shift out the remaining 7 bits. The next falling edge of BCLKX disables DX into the tri-state mode. (For 64 KHZ operation FSX must be low for 1000 ns minimum). FSX and FSR must change state only during BCLKX and BCLKR low. After a rising edge of FSR the PCM word will be latched in the receive register with the next 8 falling edge of BCLKR (BCLKX synchronous mode).

DETECTION OF LONG OR SHORT FRAME

Upon power up a short frame operation is assumed. FSX is then used to determine whether short or long frame is used.

SIGNALING

SHORT FRAME SIGNALING

In short frame signaling mode, the combo inserts a signaling bit in place of the LSB of the PCM word and extracts it from the receive side. The signaling bit is provided by SIGX input and appears at SIGR output. The combo senses a signaling frame when a FSX (FSR receive) of 2 bit clock long is applied. The decoder compensates the loss of LSB by setting the LSB to 1/2 to minimise noise and distortion.

LONG FRAME SIGNALING

The long frame signaling mode is similar to the short frame except that the combo senses a special SFX (SFR for receive) input. SFX and SFR must change state during bit clock low. SFX (SFR) high during FSX (FSR) high indicates a signaling frame.

SIGNALING ON 5552

Only short frame signaling is available on 5552.

SIGNALING ON 5553

Both short frame and long frame signaling are available on 5553. But for short frame signaling SFX and SFR must be tied low or left open circuit.

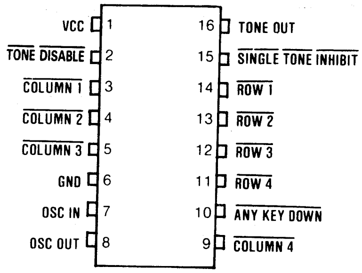
HC-5589
DTMF GENERATOR

Features

- MINIMUM EXTERNAL PARTS COUNT.
- LOW POWER CMOS CIRCUITRY ALLOWS DEVICE POWER TO BE DERIVED DIRECTLY FROM THE TELEPHONE LINE.
- USES STANDARD TV CRYSTAL (3.58 MHz) TO DERIVE ALL FREQUENCIES THUS PROVIDING VERY HIGH ACCURACY AND STABILITY.
- DUAL TONE AS WELL AS SINGLE TONE CAPABILITY.
- TOTAL HARMONIC DISTORTION BELOW INDUSTRY SPECIFICATION.
- TONE DISABLE ALLOWS "ANY-KEY-DOWN" OUTPUT TO FUNCTION FROM KEYBOARD INPUT WITHOUT GENERATING TONES.
- SPECIFICALLY DESIGNED FOR ELECTRONIC TELEPHONE APPLICATIONS.
- DIRECT REPLACEMENT FOR MOSTEK MK 5089 TONE GENERATOR.

Pin out

TOP VIEW

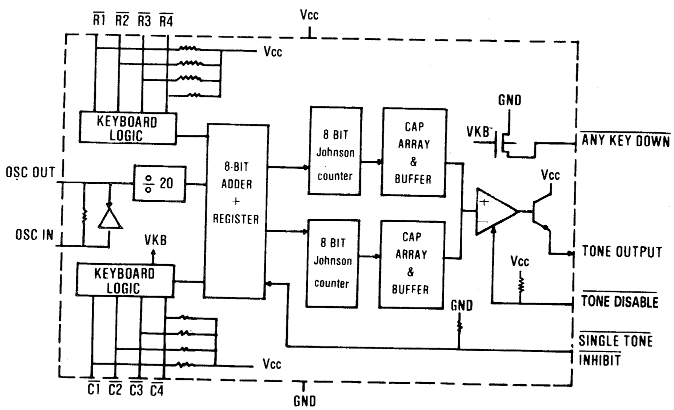


Description

The HC5589 digital tone generator is specifically designed to implement a dual tone telephone dialing system. The device interfaces directly to a standard pushbutton telephone keyboard or electronic controller and operates directly from the telephone line. All necessary dual-tone frequencies are derived from the widely used standard TV crystal providing very high accuracy and stability.

D-to-A conversion is accomplished on-chip by a capacitive network. The tone output is a stairstep image of a sine wave with very low total harmonic distortion. The output operational amplifier mixes the low and high group signals. Frequency-stability of this type of tone generation is such that no frequency adjustment is needed to meet standard DTMF specifications.

Functional diagram



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ABSOLUTE MAXIMUM RATINGS

Supply voltage Vcc	10,5 V
Input or output voltage applied	GND − 0,3 V Vcc + 0,3 V
Storage temperature	− 55° C to + 150° C
Max power dissipation	500 mW @ 25° C derate 9 mW/° C

OPERATING RANGE

Operating supply voltage	3 to 10 V
Operating temperature Range	$-30°\ C \leqslant T_A \leqslant 70°\ C$

ELECTRICAL CHARACTERISTICS (all voltages referred to GND = OV)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
Vcc	Supply voltage	3		10	V	
VIL	Input "0"	0		0,3 Vcc	V	
VIH	Input "1"	0,7 Vcc		Vcc	V	
R1	Input pull-up resistor	50		200	kΩ	
$I\overline{AKD}_{ON}$	Any-key-down sink to GND	500			µA	see note 1
$I\overline{AKD}_{OFF}$	Any-key-down off leakage			2	µA	see note 2
ICC_{OP}	Supply current operating			2	mA	see note 3
ICC_{ST}	Supply current stand-by			200	µA	see note 4
Vout	Tone output	− 10		− 7	dBm	see note 5
P-E	Pre-Emphasis, High Band	2.4	2.7	3	dB	
Trise	Rise Time			5	ms	see note 6
VNKD	Tone Output No key down			− 80	dBm	
DIST	Total output distortion			− 26	dB	see note 7
SPUR	Single Frequency spurious			− 30	dB	see note 8

NOTES :
1. Vcc = 3,5 V, VOL_{AKD} = 0,5 V
2. Vcc = 10 V, VOH_{AKD} = 10 V
3. Vcc = 3,5 V, one key depressed Outputs unloaded
4. Vcc = 10 V, $\overline{STI}$ = "0", $\overline{TD}$ = "1" no keys activated
5. Single tone, low-group 3,4 V $\leqslant$ Vcc $\leqslant$ 3,6 V 0dBm = 0,775 Vrms RLOAD = 10 kΩ
6. Time from a valid key stroke with no bounce to allow wave to go from minimum to 90 % of final magnitude of either frequency.
   Crystal parameters : RS $\leqslant$ 100Ω, LM = 96 mH CM = 0,02 pF, Ch = 5 pF, f = 3,579545 MHz, CL = 18 pF
7. Total output distortion measured in terms of out-of-tone power (0-10 kHz) to RMS sum of row and column fundamental power.
8. Relative to column level 3 V $\leqslant$ Vcc $\leqslant$ 10 V (0-10 kHz).

Oscillator

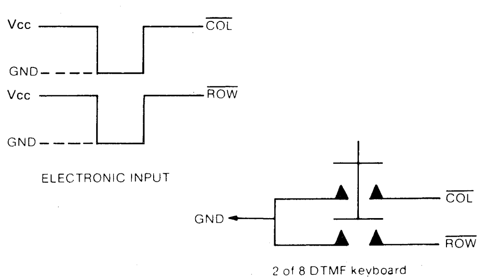
The HC5589 contains an oscillator circuit with the necessary parasitic capacitances and feedback resistor on chip so that it is only necessary to connect a standard 3.58 MHz TV crystal across the OSCin and OSCout terminals to implement the oscillator function. The oscillator functions whenever a column input is activated. The reference frequency is divided by 20 and then drives the frequency synthesizer. Frequencies are given in table 1.

TABLE 1

Standard DTMF (Hz)		Tone Output frequency using 3.59545 MHz Crystal	% Deviation From standard
F1	697	699.1	+ 0.30
F2	770	764.7	− 0.69
F3	852	852.06	+ 0.007
F4	941	939.4	− 0.16
F5	1209	1201.6	− 0.61
F6	1336	1332.7	− 0.24
F7	1477	1485.6	+ 0.58
F8	1633	1638.6	+ 0.34

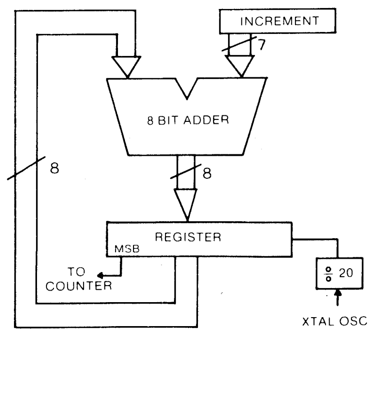
Keyboard interface

Each keyboard input is standard CMOS with a pull-up resistor to Vcc, low level on a row and a column input corresponds to a key closure. The HC 5589 can interface a standard telephone keyboard or can be controlled by open collector TTL or standard CMOS (operated off same supply as the HC 5589).



Tone generation

The HC 5589 uses a special technique to generate precise tone frequencies. For each frequency an increment is added and accumulated in a register, the most significant bit of this register is used as clock frequency for the Johnson counter which drives the capacitive digital to analog converter. Increment is choosen in order to have 16 consecutive clock matching tone periods within less than 1 %. This technique allows high oscillator division range ınd thus low frequency operation and low power consumption, the 8-bit adder is multiplexed to generate row and column tones. Oscillator division range and increment are choosen for high accuracy and low distortion.



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Dual tone mode

When one row and one column are selected, dual tone output consisting of the appropriate low group and high group tone is generated. If two digit keys that are not either in the same row or in the same column are depressed, the dual tone mode is disabled and no output is provided.

Single tone mode

Single tones either in the low group or the high group can be generated as follows. A low group tone can be generated by depressing two digit keys in the appropriate row. A high group tone can be generated by depressing two digit keys in the appropriate column, i.e., selecting the appropriate column input and two row inputs in that column.

Inhibiting single tones

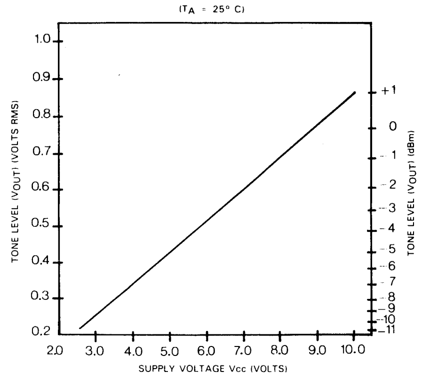
The $\overline{STI}$ input (pin 15) is used to inhibit the generation of other than dual tones. It has an internal pull down to GND supply. When this input is left unconnected or connected to GND, single tone generation as described in the preceding paragraph (single tone mode) is suppressed with all other functions operating normally. When this input is connected to Vcc supply, single or dual tones may be generated as previously described (single tone mode, dual tone mode).

Tone output

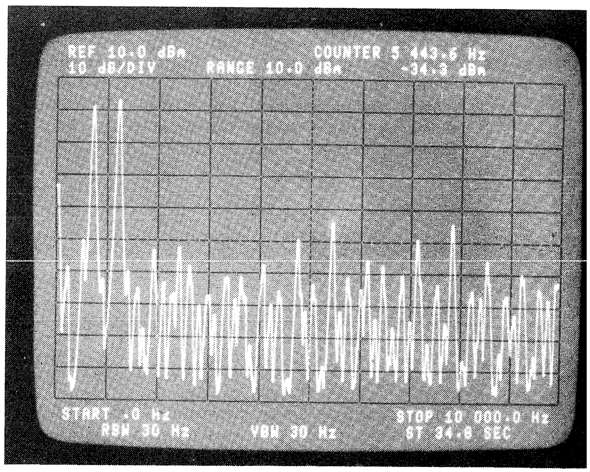
Tones are generated by two capacitive networks driven by the row and column Johnson counters. Tone level tracks power supply accurately by capacitive weighting over the whole temperature range, output level is optimised for 3,5 V operation. Tone output is connected internally to the emitter of a NPN transistor whose collector is tied to Vcc.

Tone disable

The $\overline{\text{Tone disable}}$ input is used to defeat tone generation when the keyboard is used for other functions besides DTMF signaling. It has a pull-up to the Vcc supply and when tied to GND tones are inhibited. All other chip functions operate normally.



Typical single-row level
VS Supply voltage



Spectral analysis of a typical
dual-tone waveform

MHS product assurance 8

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1. Introduction

1.1. - STATEMENT OF SCOPE

This section establishes the detail requirements for MATRA HARRIS' circuits screened and tested under the Quality Assurance Program.

Included in this section are the Quality standards and screening methods for commercial parts which must perform reliably in the field.

1.2. - APPLICABLE DOCUMENTS

The following documents form a part of this section to the extent referenced herein and provide the foundation for Matra Harris Product Assurance Program :

MIL-M-38510D	"General Specification of Microcircuits"
MIL-Q-9858A	"Quality Program Requirements"
MIL-STD-883D	"Test Methods and Procedures for Microelectronics"
NASA Publication 200-3	"Inspection System Provisions"
MIL-C-45662A	"Calibration System Requirements"
MIL-I-4508A	"Inspection System Requirements"
ESA/SCC 9000	"European Space Agency Specification for Microelectronics"

The MHS Reliability and Quality Manual, which is available upon request, describes the total function and policies of the organization to assure product reliability and quality. All customers are encouraged to visit the MHS facilities and survey the deployment of the Product Assurance function.

MATRA HARRIS maintains a Quality Assurance Program (QAP) using the above defined documents as a guide. This program assures compliance with the requirements and quality standard of control drawings and the requirements of this specification.

The special Military Program (SM) will also be found useful by those MATRA HARRIS' customers who must generate their own procurement specifications.

Use of the enclosed MATRA HARRIS standard test tables, test parameters and burn-in circuits will aid in reducing specification negotiation time.

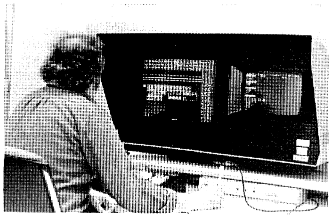
1.3. - PRODUCT ASSURANCE AT MATRA HARRIS'

Our Product Assurance department strives to assure that the quality and reliability of products shipped to customers are high quality level and consistent with customer's requirements. During product processing, there are several independant visual and electrical checks performed by Quality Assurance personnel.

Prio to shipment, a final inspection is performed at Quality Assurance plant a clearance to ensure that all requirements of the purchase order and customer specifications are met. The system and procedures used and implemented are in accordance with the latest issue of MIL-M-38510, MIL-STD-883.

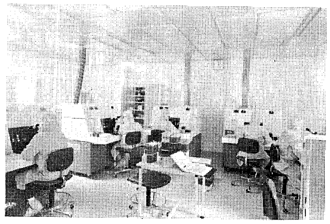
2. Product assurance operations

PRODUCT DESIGN



Quality : Parameters limits, testability
Test program control
Target specification

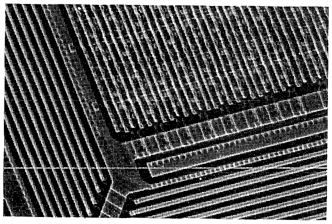
WAFER FABRICATION



Quality : Incoming inspection gate
Visual inspection
Process control

Reliability : Process qualification
Analytical test lab

PROCESS TECHNOLOGY

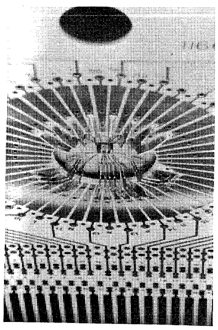


Reliability : Process qualification
Stress testing
Failure mode analysis

PACKAGE TECHNOLOGY

Reliability : Process and materials qualification
Materials tests methods
Materials characterization

PRODUCT VALIDATION/QUALIFICATION



Design Engineering : Design verification
Performance verification

Quality/Reliability : Qualification

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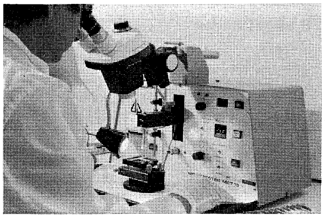
ASSEMBLY



Quality : Incoming inspection gates
Visual inspection

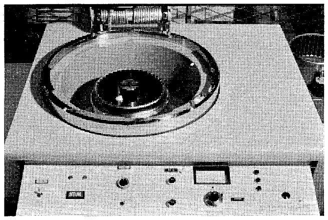
QA Acceptance

External visual	Bond pull	Physical dimension
Fine/gross leak H	Die shear	Solderability
Centrifuge	X ray	
Marking permanency	Internal visual	

Quality Monitor Program

Reliability : Process qualification

QUALITY MONITOR

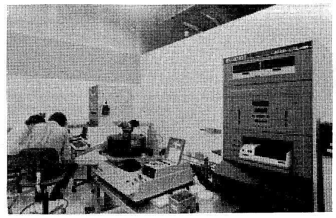


External visual	Thermal shock
Fine/gross leak H	Mechanical shock H
Lead integrity	Pressure pot P
Temp/humidity P	Moisture resistance H
Temperature cycle	

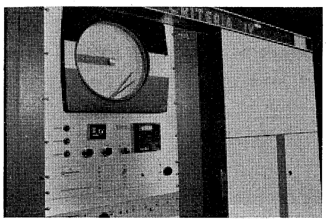
TEST AND FINISH

Quality :
Final QA acceptance
Electrical test sample
Marking permanency
External visual
Conformance to sales order

Reliability :
Reliability monitoring



RELIABILITY MONITORING

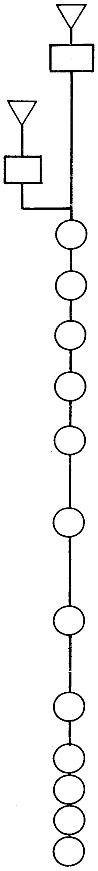


48 Hr, 125° C Burn-in
1000 Hr, 125° C Life-test

PLANT CLEARANCE

Quality : External visual
Sales order requirements

Table 1 - Wafer fabrication process flow

FLOW	PROCESS	TYPICAL ITEM	FREQUENCY	REQUIREMENTS
	Silicon wafers Incoming inspection	- Resistivity - Bow - Flatness - Taper - Oxygen content - Dimensions - Appearance	Every lot	Sampling 1 %
	Masks Incoming inspection			
	Oxidize	Thickness	Every lot	3 wafers/lot 3 points/wafer
	Implant	Resistivity C (V)	Every lot	2 wafers/lot 3 points/wafer
	Diffuse	Resistivity Thickness	Every run	4 wafers/lot 3 points/wafer
	Silicon nitride	Thickness Critical dimensions	Every lot	2 wafers/lot 5 points/wafer
	Gate oxide	Defect rates VFB Δ VFB	Every run	2 wafers/lot 2 points/wafer
	Polysilicon	- Resistivity - Thickness - Critical dimensions - Sem inspection	Every lot	5 wafers/lot 5 points/wafer
	Metallization	- Resistivity - Thickness - Critical dimensions - Sem inspection	Every run	2 wafers/run
	Passivation	- Resistivity - CVD thickness - Sem Inspection	Every run	3 points/wafer
	Test site	Electrical charact.		
	Backlap	Thickness	Every lot	1 wafer/lot
	Gold evaporation	Thickness	Every lot	1 wafer/lot
	Wafer sort	Electrical charact.	100 % chips	

2.1. - QUALITY CONTROL

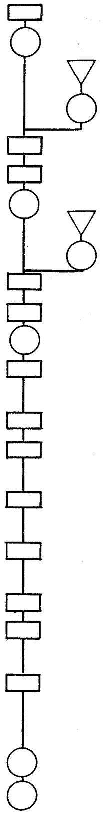
2.1.1. - Process controls

As shown by table 1 each integrated circuit shall be constructed by manufacturing processes which are under the surveillance of MHS Quality Control department. The processes shall be monitored and controlled by use of statistical techniques and computerization in accordance with published specifications and procedures. M.H.S. shall prepare and maintain suitable documentation (such as quality control manuals, inspection instructions, control charts, etc.) covering all phases of incoming part and material inspection and in — process inspections required to assure that product quality meets the requirements of this specification. The customer may verify, with the permission of and in the company of M.H.S.'s designated representative, that suitable documentation exits and is being applied. Information designated as proprietary by M.H.S. will be made available to the customer or its representative only with the written permission of M.H.S.

Process control is recognized as being vital to the concept of ''built-in'' quality. The process control program shall include a scanning electron microscope (SEM) monitor program for evaluating the metal integrity over oxide step and oxide step contour. The SEM analysis will be defined in a Quality & Reliability Assurance document.

Table 2 - QC flow charts of assembly process (I)

CERAMIC TYPE

FLOW	PROCESS MATERIALS	INSPECTION	METHOD	FREQUENCY
	Scribing	Visual	2010-6	100 %
	QC inspection	Visual	2010-6 AQL = 1.5 %	Every lot
	Lead frame, base (Incoming inspection)			
	Frame and base cleaning			
	Chip mounting			
	QC inspection	Appearance	AQL = 1.5 %	Every lot
	Wire (Incoming inspection)			
	Wire bonding	Bond strength		Every lot
	Preseal inspection	Visual		100 %
	QC inspection	Visual	AQL = 1.5 %	Every lot
	Sealing	Humidity appearance		100 %
	Stabilisation bake			
	Temperature cycling	10 cyles	1010.4 Condition C	100 %
	Fine leak		1014 Condition A or B	100 %
	Gross leak		1014 Conditions C	100 %
	Plating			
	Plating inspection	Appearance thickness		Every lot
	Centrifuge		2001.2 Condition E	
	Lead cut			
	Marking	Permanency		Every lot
	QA final inspection		LTPD 5 Acc on 1	

2.1.2. - Control of procurement sources

M.H.S. shall be responsible for assuring that all supplies and services conform to this specifications, the detail specification and M.H.S.'s procurement requirements.

A - RECEIVING INSPECTION

Purchased supplies shall be subjected to inspection after receipt as necessary to ensure conformance to contract requirements. In selecting sampling plans, consideration shall be given to the controls exercised by the procurement source and evidence of substained quality conformance.

B - M.H.S. shall initiate corrective action with the procurement source depending upon the nature and frequency of receipt of nonconforming supplies.

2.1.3. - Inspection and testing procedures coverage

Inspection and testing processes and procedures prepared in fulfillment of the reliability assurance program shall be prescribed by clear, complete and current instructions. These instructions shall assure inspection and test of materials, work in process and completed integrated circuits as required by this specification. In addition, criteria for approval and rejection of materials and integrated circuits shall be included.

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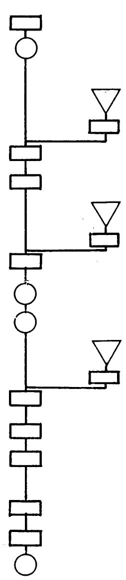
Table 3 - QC flow charts of assembly process (RI)

PLASTIC PACKAGE

FLOW	PROCESS/MATERIALS	METHOD/TEST	FREQUENCY
	Scribing	Visual inspection	Every lot
	QC visual inspection	2010-6 AQL = 1.5 %	Every lot
	Lead frame (Incoming inspection)		
	Frame cleaning		
	Chip mounting		
	Wire (Incoming inspection)		
	Wire bonding	Bond strength	Every lot
	Premold inspection		100 %
	QC lot acceptance	AQL 1.5 % L II	Every lot
	Mold compoud (Incoming inspection)		
	Molding		
	Post mold bake		
	Tin plate	Appearance thickness	Every lot
	Lead cut and bending		
	Marking	Permanency	Every lot
	QA final inspection	LTPD 5/Acc = 1	Every lot

2.1.4. - Inspection records

M.H.S. shall maintain a reliability data and records library. This library shall have on file, for review by the procuring activity, records of examination, qualification test results, variables data (when required) and all other pertinent data generated on devices manufactured to this specification.

TABLE 4 - Groupe A : inspection (for MHS processed products)

Subgroup		AQL	Inspection level
1	Visual and mechanical inspection	0.4 % major defect	II
2a	Inoperative (at 25° C and high temperature)	0.1 %	II
	At low temperature	0.4 %	II
2b	Parametric (at 25° C and high (temperature)	0.1 %	II
	At low temperature	0.4 %	II
2c	Dynamic (worst case testing conditions Voc min, Vih min, Vil max)	0.1 % at 25 % & high temp.	II
		0.4 % at low temp.	II

A single sample may be used for all subgroup testing. Where the required size exceeds the lot size, 100 % inspection shall be allowed.

3. - Qualification and quality conformance inspection

3.1. - GENERIC FAMILY DEFINITION

Electrically and structurally similar devices shall be said to comprise a generic family (e. g. CMOS) if they meet the following criteria :

A - Are designed with the same basic circuit-element configuration such as CMOS, MOS silicon-gate, and differ only in the number of complexity of specified circuits which they contain.

B - Are designed for the same supply, bias and signal voltage, and for input/output capability with each other under an established set of loading rules.

C - Are enclosed in housings (packages) of the same basic construction (e. g., hermetically sealed flat packages, dual-in-line ceramic, dual-in-line plastic) and outline, differing only in the number of active housing terminals included and/or utilized.

3.2. - QUALITY CONFORMANCE INSPECTION

Quality conformance inspection group B, C and D requirements are per table 5, 6 and 7.

A - When specifically called out and funded on the purchase order or contract, M.H.S. shall perform quality conformance inspections (group C and/or D) on a lot-by-lot basis.

3.4. - GROUP A CONFORMANCE (TABLE 4)

Group A conformance shall consist of the electrical parameters in M.H.S. data sheet. If an inspection lot is made up of a collection of sublots, each sublot shall conform to group A, as specified.

Subgroup :

Subgroup 2a	25° C, dc and ac
Subgroup 2b	High temperature, dc and ac
Subgroup 2c	Low temperature, dc and ac.

3.5. - CERTIFICATION

The M.H.S. shall include a certificate of compliance with each shipment of parts if requested on the purchase order. This certificate shall indicate that all specified tests and requirements of this specification have been made or met, and that the lot of devices (identified by lot and/or batch number) is acceptable. The certificate shall bear the name and signature of M.H.S. Quality Control representative, the date of acceptance or signing, and any pertinent notes as applicable.

EVERY LOT — Table 5 - Group B : lot acceptance

TEST DESCRIPTION	TESTS CONDITIONS MIL STD 883 B	SAMPLE SIZE	LTPD	ACC ≠	REMARKS
External visual	Method 2009-2	15	15	0	
Radiography	Method 2012-3	15	15	0	
Physical dimensions	Method 2016	5	50	0	
Tin plating thickness		5	50	0	
Marking permanency	Method 2015-2	5	50	0	
Internal visual	Method 2010-6	5	50	0	
Bond strength	Method 2011 -3	5	50	0	No wire ⩽ 2,5 gr
Die shear Strength	Method 2019 -1	5	50	0	⩾ 5 kg
Seal fine leak gross leak	Method 1014 condition A Method 1014 condition C	77 77	5 5	1 1	$\leqslant 5 \times 10^{-8}$ At s/cc
Solderability	Method 2022 $\theta = 240° C \pm 5° C$	5	50	0	Visual inspection is also performed according to Method 2003

EVERY TWO MONTHS — Table 6 - Group C : die related tests

	TEST DESCRIPTION	TEST CONDITIONS	SAMPLE SIZE	LTPD	ACC ≠	REMARKS
SUBGROUP 1	Temperature cycling	Method 1010 condition C 100 cycles	77	5	0	End point Electrical Visual
	Constant acceleration* 1	Method 2001 condition E	77	5	0	End point Electrical & Visual
	SEAL* 1 Fine leak Gross leak	Method 1014 condition A Method 1014 condition C	77 77	5 5	1 1	
	Internal visual	Method 2013	15	15	0	
SUBGROUP 2	Operating life test	Method 1005	77	5	1	Interim read out 24, 48, 96, 168, 500 and 1000H
	High temperature storage	Method 1008 -1 Hermetic condition D Plastic condition C	77	5	1	End point Electrical &

* 1 hermetic package only

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EVERY THREE MONTHS Table 7 - Group D : package related tests

	TEST DESCRIPTION	TEST CONDITIONS	SAMPLE SIZE	LTPD	ACC	REMARKS
SUGROUP 1	Lead integrity Tension Fatigue Torque	Method 2004 2 condition A condition B2 condition C1	15	15	0	
	Seal a) fine b) gross	Method 1014 condition A condition C	15	15	0	
SUBGROUP 2	Thermal shocks	Method 1011 condition C 15 cycles	77	5	1	End point Electrical & Visual
	Temperature cycling	Method 1010 condition C 100 cycles	77	5	1	
	85° C / 85 % / RH	1000 H	77	5	1	Interim read out 48, 168, 500, 1000 H
	Pressure pot* 2	125° C 2 atm 96 H	77	5	1	Interim read out 24, 48, 96 H
	Seal* 1	Method 1014				
	a) fine		77	5	1	
	b) gross		77	5	1	
	External visual	Method 2009	77	5	0	
SUBGROUP 3	Mechanical shock	Method 2002	15	15	0	
	Constant acceleration* 1	Method 2001 condition E	77	5	1	End point Electrical & Visual
	Seal* 1					
	a) fine		77	5	1	
	b) gross		77	5	1	
	Internal visual		15	15	0	
	Bond strength		15	15	0	
	Die shear strength		15	15	0	
SUBGROUP 4	Salt fog	Method 1009 condition A	15	15	0	End point Electrical Visual and Seal

* 1 : hermetic package only
* 2 : plastic package only

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M.H.S. STANDARD FLOWS

OPERATIONS	COMMERCIAL – 5 0° C ; 70° C	INDUSTRIAL – 9 –40°C ; +85°C	MILITARY – 2 –55°C ; +125°C
1 Referenced norm or standard	MIL STD 883 C	MIL STD 883 C	MIL STD 883 C
2 Particular spec applicable	Data sheet	Data sheet	Data sheet
3 Traceability	wafer lot number on parts	wafer lot number on parts	wafer lot number on parts
4 Products incoming and wafer fab	as applicable	as applicable	as applicable
5 Electrical testing and probe	100 % 25° C	100 % 25° C	100 % 25° C
6 Assembly internal level and location	level 4 (plastic) level 7 (hermetic) Dynetics	level 7 level 4 level 3 Dynetics	level 3 Dynetics HSM
7 Piece parts traceability	Applicable	Applicable	Applicable
8 Die prepand inspection	100 % MHS spec	100 % MHS spec	100 % Méth. 2010 B
9 Assy screening after sealing - Stabilization bake - Temperature cycling (–65° C ; +150° C) - Centrifuge - Fine and Gross leak - Open/short test - Visual Inspection (external)	 24 H 150° C 10 cycles (hermetic only) 100 % 100 % (hermetic only) 100 % 100 %	 24 H 150° C 10 cycles 100 % 100 % 100 % 100 %	 24 H 150° C 10 cycles 100 % 100 % 100 % 100 %
10 Incoming of devices from far east sampling test - External visual - Physical dimensions - X Ray inspection - Resistance to solvent - Hermeticity - Temperature cycling (15 cycles) - Solderability - Internal visual - Bond pull and die shear	 LTPD 15 LTPD 50 LTPD 15 LTPD 50 LTPD 5 (hermetic only) LTPD 5 (hermetic only) LTPD 50 LTPD 50 LTPD 50	 LTPD 15 LTPD 50 LTPD 15 LTPD 50 LTPD 5 LTPD 5 LTPD 50 LTPD 50 LTPD 50	 LTPD 15 LTPD 50 LTPD 15 LTPD 50 LTPD 5 LTPD 5 LTPD 50 LTPD 50 LTPD 50
11 Final test - Pre burn-in test - Burn-in (150° C) New products only - Final electrical test - PDA check - Marking - Final quality control (all lots) • group A • ext. visual insp.	 25° C DC + FLF 24 H 125° C AC + DC 10 % MHS spec LTPD 5 LTPD 15	 25° C DC + FLF 24 H 125° C AC + DC 10 % MHS spec LTPD 5 LTPD 15	 25° C DC + FLF 24 H 125° C AC + DC 10 % MHS spec LTPD 5 LTPD 15
12 Lots qualification (periodic tests) - Group B - Group C - Group D	 required required required	 required required required	 required required required

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MILITARY AND HIGH RELIABILITY FLOWS

COMPARISONS BETWEEN MILITARY AND HI-REL FLOWS

OPERATIONS	MILITARY – 8	MILITARY SEMI-CUSTOM FLOW S M	HI-REL S H
1 Referenced norm or standard	MIL STD 883 B2	MIL STD 883 B with option for customers	ESA/SCC 9000
2 Particular applicable spec	Data sheet	Customer spec	SCC spec or customer spec
3 Traceability	wafer lot number on parts	All operations lot by lot	SCC spec or customer spec
4 Products incoming and wafer fabrication	as applicable	as applicable	as applicable
5 SEM inspection	NA	Upon customer request	Required per SCC 21400
6 Electrical testing and probe	100 %	100 %	100 % with wafer selection
7 Die prep and inspection	100 % method 2010 condition B	100 % method 2010 condition B	100 % method 2010 condition A
8 Assembly level and location	level 3 HSM Dynetics	level 3 HSM Dyneticss	level 2 Nantes
9 Piece parts traceability	Applicable	Applicable	Required
10 Customer precap inspection	NA	Optional method 2010 condition B	MIL STD 883 method 2010 condition A
11 Assy screening after sealing - Stabilization bake - Temperature cycling (−65° C ; +150° C) - Centrifuge (30 000 G) - Fine leak (method 1014 A) - Gross leak (method 1014 C) - Open/short test - Visual Inspection (ext.)	 24 H 150° C 10 cycles 100 % 100 % 100 % 100 % 100 %	 24 H 150° C 10 cycles 100 % 100 % 100 % 100 % 100 %	 24 H 150° C 10 cycles 100 % 100 % 100 % 100 % 100 %
12 Incoming of devices from far east sampling tests - Ext. visual Inspection - Physical dimensions - X Ray inspection - Resistance to solvent - Hermeticity (Fine leak & Gross leak) - Temperature cycling (15 cycles) - Solderability - Internal visual inspection - Bond pull and die shear	 LTPD 15 LTPD 50 LTPD 15 LTPD 50 LTPD 5 LTPD 5 LTPD 50 LTPD 50 LTPD 50	 LTPD 15 LTPD 50 LTPD 15 LTPD 50 LTPD 5 LTPD 5 LTPD 50 LTPD 50 LTPD 50	 NA NA NA NA NA NA NA NA NA

8

MILITARY AND HIGH RELIABILITY FLOWS

COMPARISONS BETWEEN MILITARY AND HI-REL FLOWS

OPERATIONS	MILITARY – 8	MILITARY SEMI-CUSTOM FLOW S M	HI-REL S H
13 Final test			
- Electrical tests	NA	NA	High and low temp.
- Serialization	NA	NA	Level B
- Pre burn-in test	25° C DC + FBF	25° C DC + FBF	25° C DC + FBF
- Burn-in (125° C)	168 H	168 H	168 H or 240 H
- Post burn-in test	125° C DC + AC – 55° C by sampling	25° C DC + AC 125° C DC + AC – 55° C by sampling	25° C DC + FBF –55° C & 125° C DC + AC
- Delta or PDA calculation	PDA = 10 %	PDA = 10 % if no customer request	PDA = 3 % Delta for level B
- Marking	MHS spec	Per customer spec	SCC spec
- Final quality control (all lots)			
• Group A – 25° C, 55° C, 125° C	LTPD 5	LTPD 5	NA
• Leaks	NA	NA	100 %
• X-ray	NA	NA	100 %
• External visual inspection	LTPD 15	LTPD 15	100 %
14 Lots qualification (periodic tests)			
- Group B	Required	Required	* special lot acceptance test as per SCC 9000
- Group C	Required	Required	"
- Group D	Required	Required	"
15 Customer source inspection	Applicable	Applicable	Required
16 Data base	Certificate of compliance	Per customer's request	Required (complete)

Grade Products

This product is processed on the same wafer fabrication lines, to the same thorough specification and rigid controls as HI-Rel parts. At wafer electrical probe the product may be categorized for electrical performance, such as temperature range of operation or maximum output (see specific product data sheet for grading details) by utilizing multiple colored inks. Defective die are inked with red ink, but, for example, die meeting the commercial temperature range electrical specifications may be inked with green ink.

The die are then visually inspected and sorted after die separation to class B visual criteria. They are then assembly on a domestic assembly line under stringent control.

Matra-Harris invites any interested customer to review our assembly flows and facilities for information quality survey or certification.

4. Reliability

The reliability approach at Matra-Harris Semiconductor is based on designing in reliability rather than testing for reliability only. The latter is applied to check and confirm that sound design with quality and reliability ground rules are observed and correctly executed in a new product design.

Reliability engineering becomes involved as early as concept review of a new product and continues to remain involved through design and layout reviews. At these critical development points of a new design, basic reliability layout guidelines are invoked to insure an all-around reliable design. This concept is reflected by the MHS reliability procedures which encompass mandatory first run product evaluation. This is done at not only the circuit level, but also at the process and package level. Reliability engineering approval is required before new product designs are released to manufacturing.

Both maximum rated and accelerated stress conditions are performed. Acceleration is important to determine how and at what stress level a new design would fail. From this information, necessary design changes can be implemented to insure a wider and safer margin between the maximum rated stress condition and the device's stress limitation.

4.1. - OPERATING OR STATIC LIFE TEST

Performed at 125° C accelerated testing under dynamic or static operation mode at nominal voltage is used to know the reliability of our products under accelerated temperature conditions, and bring knowledge of failure modes and mechanisms.

4.1.1. - CMOS static rams

TECHNOLOGY	DEVICE TYPE	PACKAGE	BURN-IN 48 H	LIFE-TEST READ-OUT				
				168 H	500 H	1000 H	2000 H	5000 H
SAJI IV	HM 6514 (991)	Cerdip	0/526	1/526 (1)	1/525 (2)	1/524 (3)	0/190	
,,	HM 6514 (991)	Plastic	11/2194	3/2122 (4)	0/288	1/216 (5)	0/71	
,,	HM 6504 (918)	Cerdip	1/469	0/468	2/468 (6)	0/466	0/466	
Scaled SAJI IV	HM 6504 (1298)		1/264	0/263	0/263	0/263	2/263 (7)	
,,	HM 65161 (1195, 2128)	Cerdip	6/690	2/684 (8)	1/683 (9)	2/682 (10)	0/251	
,,	HM 65161 (1195, 2128)	Plastic	0/100	0/100	0/100	0/100		

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4.1.2. - NMOS microcontrollers/microprocessors

DEVICE TYPE	PACKAGE	LIFE-TEST READ-OUT					
		48	168	500	1000	2000	5000
8048 H	Cerdip	1/450 (1)	0/450	0/450	0/450	0/450	0/450
8048 H	Plastic	1/85 (2)	0/84	0/84	0/84	0/84	0/84
8086 H	Cerdip	4/155 (3)	0/154	0/151	2/151 (4)	0/149	

Failure analysis : CMOS

(1), (2), (3) Cell failure, contamination E_A = 1 eV
(4), (5) Cell failure, contamination E_A = 1 eV
(6) Leakage E_A = 0,7 eV
Contamination E_A = 1 eV
(7) Cell failures, contamination E_A = 1 eV
(8) Test escapes
(9) Contamination E_A = 1 eV
(10) Contamination E_A = 1 eV
Input leakage

NMOS

(1) Oxide isolation failure E_A = 0,5 eV
(2) Bonding failure, design corrected
(3) 2 open, due to mismonting
2 basic functional E_A = 0,7 eV
(4) 1 open
1 basic functional E_A = 0,7 eV

4.2. - PACKAGE RELATED TESTS

The testing of packages is complementary to operating or static life testing. The reliability of the device in its package versus, the environmental conditions are tested during extended temperature humidity bias life tests, pressure cooker and temperature cycling.

The test conditions are the following :

1 - Temperature - humidity bias life-test is done at 85° C, and 85 % relative humidity. The device is static bias. The pins are alternatively high or low.

2 - Thermal cycling. Test of mechanical stress in the package. We use the MIL-STD 883 method 1010 condition C (– 65° C, + 150° C) (method of the two chambers).

3 - Pressure cooker. Used for internal evaluation T = 121° C, P = 2 atms.

TESTED DIES	TEMPERATURE HUMIDITY BIAS TEST 85° C/85/RH 1000 H	THERMAL CYCLING METHOD 1010 MIL-STD 883 CONDITION C – 65° C/H 50° C 1000 CYCLES 50 MM/CYCLES
6514 18 leads 0.3 cerdip	N/A	0/100
6514 18 leads 0.3 plastic	1/100	0/100
65161 24 leads 0.6 cerdip	N/A	0/100
65161 24 leads 0.6 plastic	0/100	0/100
8048 40 leads 0.6 cerdip	N/A	0/100
8048 40 leads 0.6 plastic	4/105	1/100

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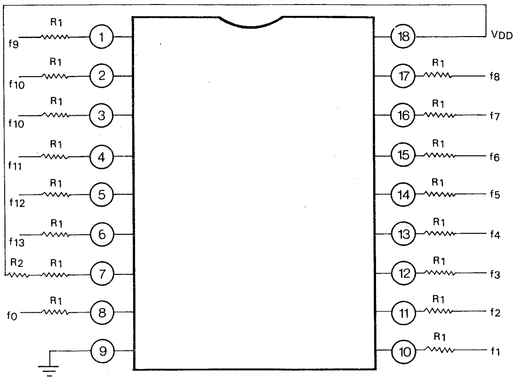
4.3 - BURN-IN DIAGRAMS

HM 6504



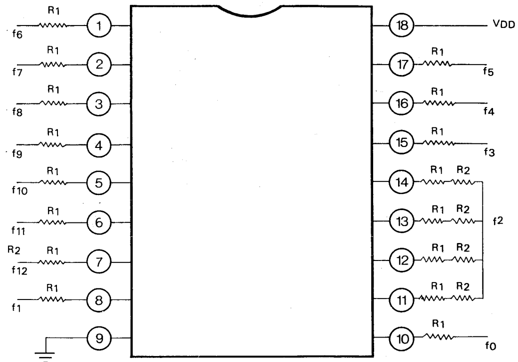
R_1 = 300 Ω + or − 5 % 1/4 W per socket = 16

R_2 = 2 KΩ + or − 5 % 1/4 W per program card = 1
per 190 sockets à f_0 = 100 KHz + ou − 20 %

$f_n = f_n - 1/2$

V_{dd} = 5,0 V + 0,5 V
− 0,0 V

HM 6514

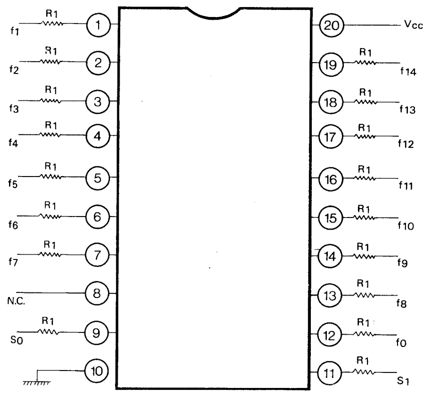


R_1 = 300 Ω + or − 5 % 1/4 W per socket = 15

R_2 = 2 KΩ + or − 5 % 1/4 W per program card = 4
per 190 sockets à f_0 = 100 KHz + ou − 20 %

V_{dd} = 5,0 V + 0,5 V f_n − 1/2
− 0,0 V

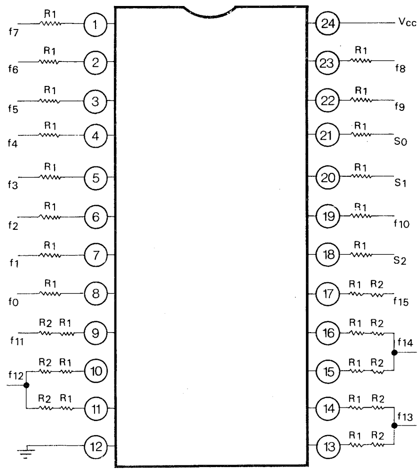
HM 65261



R_1 = 300 Ω (+/− 5 %) 1/4 W

V_{cc} = 5,0 V (+ 0,5 V / − 0,0 V)

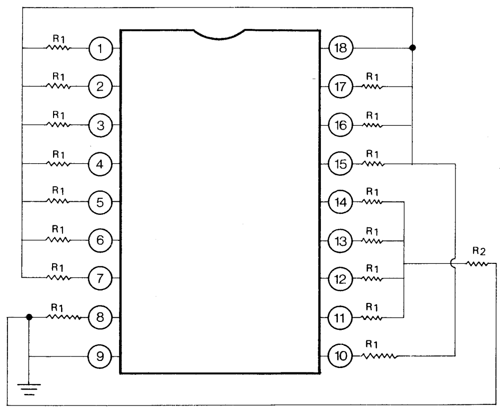
HM 65161



R_1 = 220 Ω per row : 22 R_2 = 2,2 KΩ per program card : 8

V_{cc} = 5,0 V (+ 0,5 V/− 0,0 V)

HM 6561

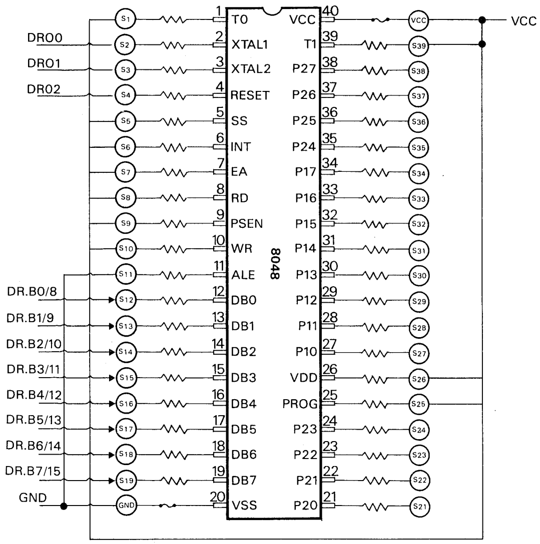


R_1 = 300 Ω + or − 5 % 1/4 W per socket = 16

R_2 = 2 KΩ 1/4 W per program card = 1

V_{cc} = 5,0 V + 0,5 V
− 0,0 V

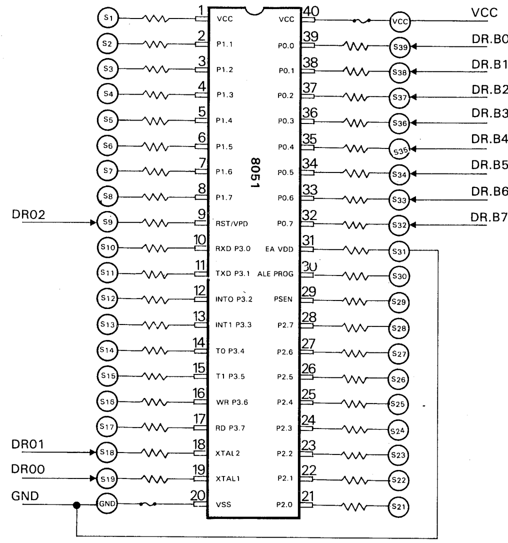
8048/8035



VCC = 5,0 V (+ 0,5 V/– 0,0 V)

R = 1 KΩ 1/4 W une par circuit

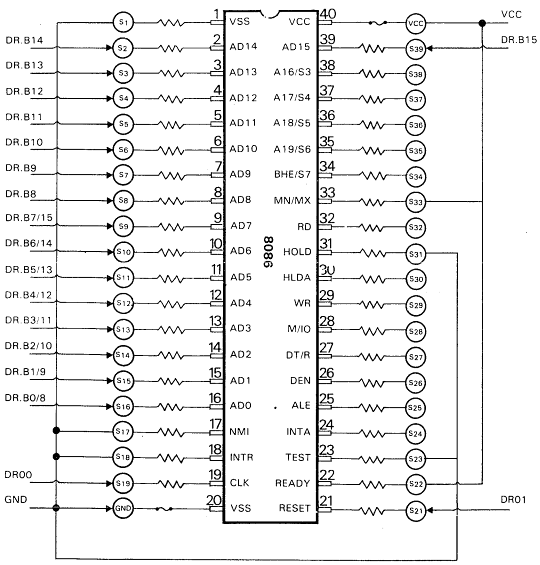
8051/8031



VCC = 5,0 V (+ 0,5 V/– 0,0 V)

R = 1 KΩ 1/4 W une par circuit

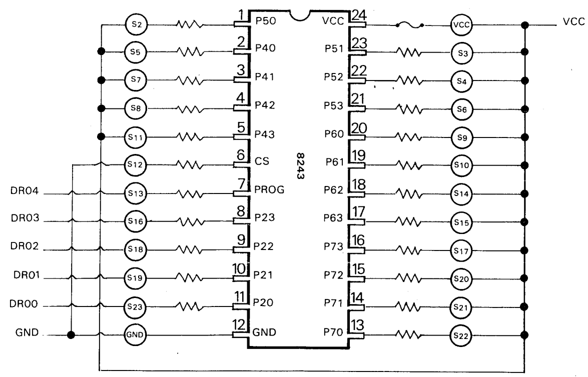
8086



VCC = 5,0 V (+ 0,5 V/– 0,0 V)

R = 1 KΩ 1/4 W une par circuit

8243/C43



VCC = 5,0 V (+ 0,5 V/– 0,0 V) : f = 500 KHz

R = 220 Ω 1/4 W une pour 18 circuits

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Ordering & packaging 9

9

Component Ordering Information

● Memories and telecommunication circuits

H M 1 - 65261 B - 2

PREFIX
H -

FAMILY
C - Communication
M - Memory

PACKAGE CODE
0 - Chip Form
1 - Ceramic
3 - Epoxy
4 - Leadless Carrier
5 - Substrate and leadless assembly

DEVICE TYPE

TEMPERATURE
2 - − 55° C to + 125° C
5 - 0° C to + 70° C
6 - 100 % 25° C Probe
8 - Dash 8 Program
Mil Std. 883B
9 - − 40° C to + 85° C

VERSION*
CMOS
B - High speed - Low power
C - Relaxed version
Blank - Standard product
S - High speed - High power

* All versions may not be applicable to every product
Check data sheet

● Microprocessors

M D 8086 /B

• **TEMPERATURE RANGE**
- BLANK : Commercial (only one character before device type)
- I : Industrial − 40° C + 85° C
- M : Military − 55° C + 125° C
- X : Dice probed at 25° C only

• **PACKAGE TYPE**
- C : Side brazed
- D : Cerdip
- G : Pin grid
- P : Plastic
- R : Leadless chip carrier
- X : Dice form

• **DEVICE TYPE**

• **MISCELLANEOUS**
- Speed : − 2, − 1
- Mil cond. B:/B
- Rom code for microcontrollers only : ••

EXAMPLES :
P-8031 : Standard plastic 8 bit microcontroller ROMless - Commercial temperature range
ID-8086 : Industrial temperature range (− 40° C + 85° C) for 8086 - 5 MHz - Cerdip package
XX-80C48 : Dice probed at 25° C - packaged in chip-tray
D-8086-2 : 8086 in cerdip - 8 MHz
MD - 8031/B : 8031 after mil std. 883 - cond. B
Military temperature range (− 55° C + 125° C)
Burn-in 168 H.

● Gate arrays

M A 1 C — 1200 A05 — 2

PREFIX
MHS

FAMILY
HIGH SPEED
GATE ARRAY

PACKAGE CODE
0 - Chip Form
1 - Ceramic
3 - Epoxy
4 - LCC

PIN COUNT
« space » - 24

A - 8
B - 14
C - 40
D - 64
E - 16
F - 18
G - 20
H - 22
I - 28
J - 32
K - 48

GATE COUNT
0250
0400
0800
1200

Customer
Specification

TEMPERATURE
2 : − 55° C to + 125° C
5 : 0° C to + 70° C
6 : 25° C probe
9 : − 40° C to + 85° C

Wafer form code

DW 1200 A05

↑

0250
0400
0800
1200

PACKAGE OPTIONS	LEAD COUNT	MA 0400 MA 0250	MA 0800	MA 1200
PLASTIC DIL	8	X		
	14	X		
	16	X		
	18	X		
	20	X		
	22	X	X	
	24	⊗	⊗	⊗
	28	X	X	X
	40	⊗	⊗	⊗
CERAMIC DIL	18	X		
	20	X		
	22	X	X	
	24	⊗	⊗	⊗
	28	X	X	X
	40	⊗	⊗	⊗
	48 (Side Braze)		X	X
	64 (Side Braze)			X
LCC	28	⊗		
	32	X	⊗	
	40	⊗	⊗	⊗
	48		⊗	X
	64		X	⊗

NOTE 1 : Standard package (a stock is built on such packages in Nantes) = ⊗
Non-standard package (final customer has to inform MHS enough in advance in order to build corresponding piece part stock) = X
NOTE 2 : Prototypes will be delivered in side brazed package (Nantes assembly)
NOTE 3 : For other packages, contact your nearest MHS sales office or representative

● **Special orders**

For best availability and price, it is urged that standard ''Product Code'' devices be specified, which are available worldwide from authorized distributors. Where enhanced reliability is needed, note standard ''Dash 8'' screening described in this Data Book. MHS application engineers may be consulted for advice about suitability of a part a given application.

If additional electrical parameter guarantees or reliability screening are absolutely required, a Request for Quotation and Source Control Drawing should be submitted through the local MHS Sales Office or Sales Representative. Many electrical parameters cannot be economically tested, but can be assured through design analysis, characterization, or correlation with other parameters which have been tested to specification limits. These parameters are labeled ''sampled and guaranteed but not 100 % tested''.

MHS reserves the right to decline to quote, or to request modification to special screening requirements.

Package Selection Guide

	CERDIP	EPOXY	LCC
MEMORY AND COMMUNICATION IC CODE	1	3	4
MICROPROCESSOR CODE	**D***	**P***	**R****
RAM memory			
HM 6116	5F	7G	LU
HM 6504	5E	3D, 3T, 7D	LB
HM 6514	5E	3D, 3T, 7D	LB
HM 65161	5F	7G	LU
HM 65261	C1	3N	L08
HM 6561	4N	3D, 3V	LA, LB
HM 6564		Leadless Array Package MA	
HM 65681	C1	3N	L08
HM 6816 A	5F	7G	L07
Microprocessor			
8031	C4	3H	44 pins, type C
8035 HL	5H	3H	''
8048 H	5H	3H	''
8051	C4	3H	''
8086	C4	—	''
8088	5H	3H	''
80C35	C4	3H	''
80C48	C4	3H	''
82C43	4K	7G	''
Telecommunications IC			
HC 5510	4K, C5	—	—
HC 5512	CO, C7	—	—
HC 5557	CO, C7	—	—
HC 5589	—	3L, K5	—

NOTE : * These package numbers has to be used in product ordering

** Contact factory for latest availability of devices in these packages

NOTE FOR PACKAGE DRAWNINGS ON FOLLOWING PAGES

1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ± .010 (± 0.25 mm) unless otherwise shown.
3. Internal package codes are shown in black squares.

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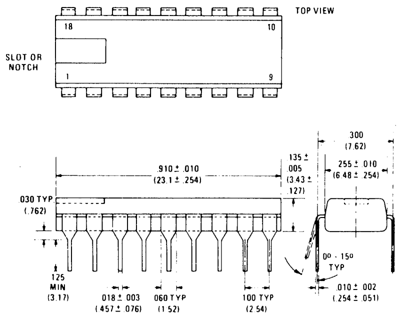
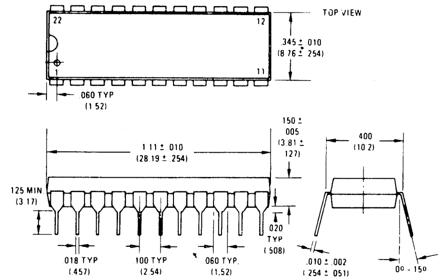
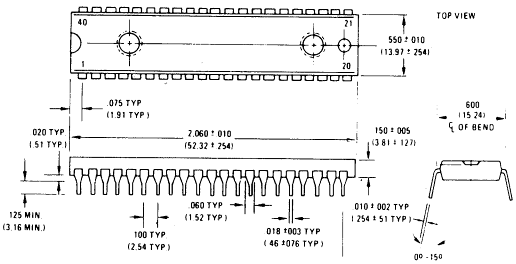
3D 3T 3V 7D 18 LEAD EPOXY DIP



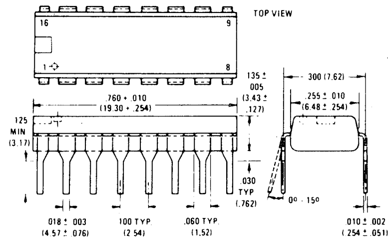
3F 7G 22 LEAD EPOXY DIP



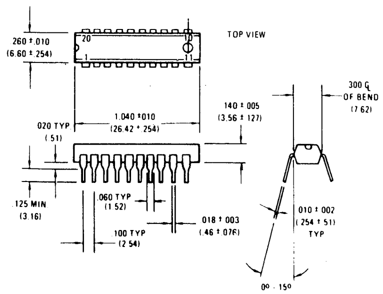
3H 40 LEAD EPOXY DIP



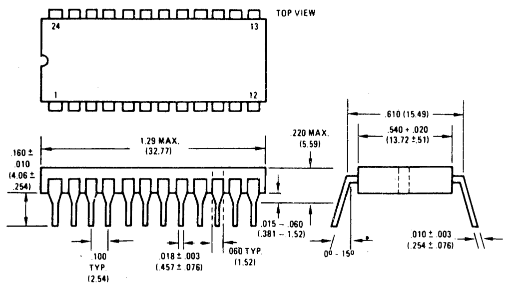
3K 3L K5 16 LEAD EPOXY DIP



3N 20 LEAD EPOXY DIP



4K 5F 24 LEAD CERDIP



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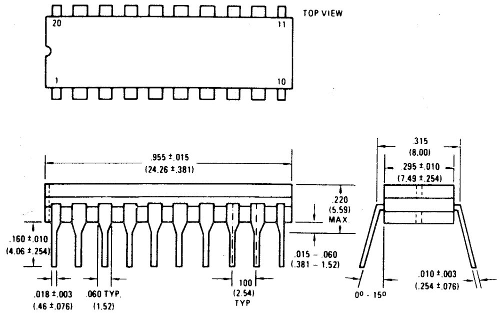
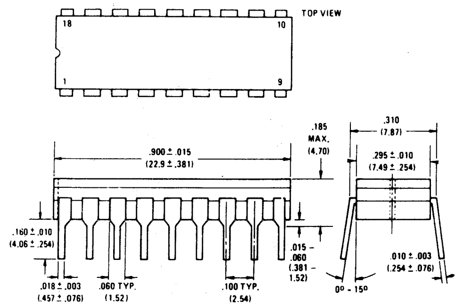
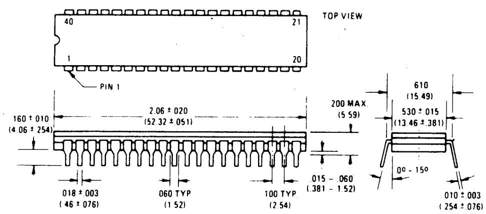
4L C1 — 20 LEAD CERDIP



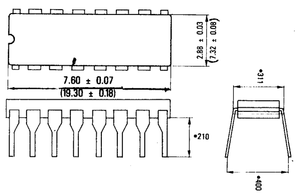
4N 5E — 18 LEAD CERDIP



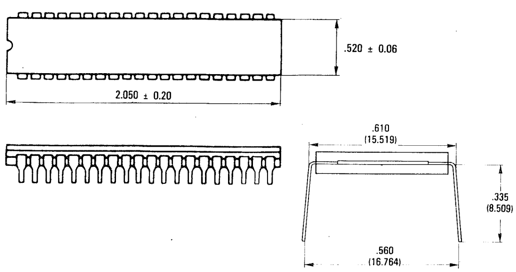
5H — 40 LEAD CERDIP



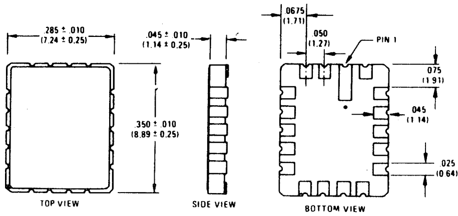
C0 — 16 LEAD CERDIP



C4 — 40 LEAD CERDIP



LA LB — 18 LEAD LEADLESS CHIP CARRIER



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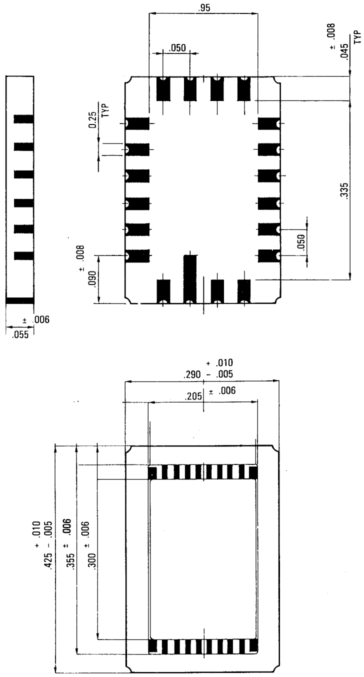
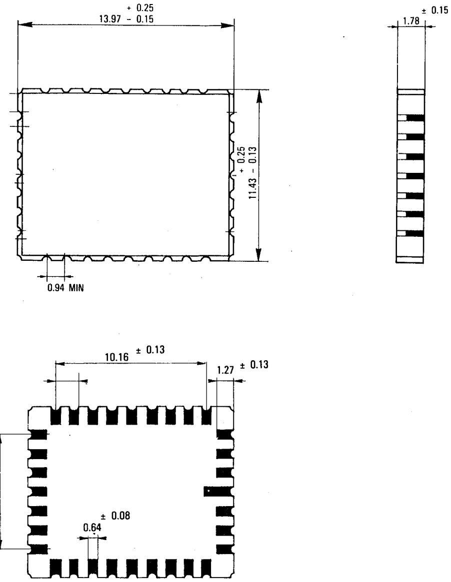
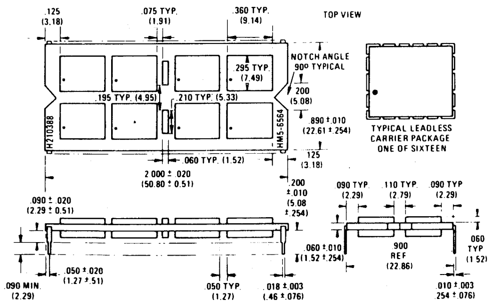
L08 20 LEAD LEADLESS CHIP CARRIER



LU 32 LEAD LEADLESS CHIP CARRIER



MA 40 LEAD 64K RAM MEMORY MODULE



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Order form for mask programmable parts 10

ORDER FORM FOR MASK PROGRAMMABLE PARTS

Company :
Name address

Company contact : Phone :
P.O. ≠ :
Date :

Package type ... Plastic (DIL)
... Cerdip (DIL)

Temperature range ... 0° C + 70° C
... − 40° C + 85° C
... − 55° C + 125° C

Burn in ... No
... Yes

Quality level ... Standard
... Special

RESERVED FOR MHS USE
MHS P/N

PM Appr. :
Date :

PE Appr. :
Date :

CAD Appr. :
Date :

MARKING

Marking will consist of a Matra Harris Logo, product and package type, the 2 digits Matra Harris pattern number, a data code and customer part number (limited to a maximum of 9 digits or spaces).

PROGRAMMING INFORMATION (to be sent per format described in Matra Harris programming instruction brochure).

Customer part number

Physical support : ... Master device (2716, 2732, 2764, 8748, 8751, 8048, 8051...) Type ______

... Floppy disk
Disk name
Density ... Single ... Double (1)

... I/O Option : ... TTL ... CMOS
Blank devices to be programmed (1)
... No
... Yes Type ______

Quantities ...
Standard : 25 pcs
Special : ....

VERIFICATION MEDIUM : THE CUSTOMER WILL BE SENT ONE OR MORE OF THE FOLLOWING MEDIA TO VERIFY MHS RECEPTION OF VALID DATE, IF ANY EPROM IS SELECTED, BLANCK EPROMS MUST BE SUBMITTED WITH THIS FORM.

CIRCLE ONE OR MORE :

LISTING HEXADECIMAL FORM
VERIFICATION FORM

EPROM : 2716 - 2732 - 2764

10

(1) consult M.H.S.

Dice information 11

11

Dice Ordering Information

GENERAL INFORMATION

MHS Memory Products are available in chip form to the hybrid micro circuit designer. The standard chips are DC electrically tested at + 25° C to the data sheet limits for the commercial device and are 100 % visually inspected to MIL-STD-883, Method 2010, Condition B criteria. Packaging for shipment consists of waffle pack carriers plus an anti-static cushioning strip for extra protection.

The hybrid industry has rapidly become more diversified and stringent in its requirements for integrated circuits. To meet these demands MHS has several options additional to standard chip processing available upon request at extra cost. For more information consult the nearest MHS Sales Office.

CHIP ORDERING INFORMATION

Standard and special chip sales are direct factory order only. Contact the local MHS Sales Office for pricing and delivery on special chip requirements.

MECHANICAL INFORMATION

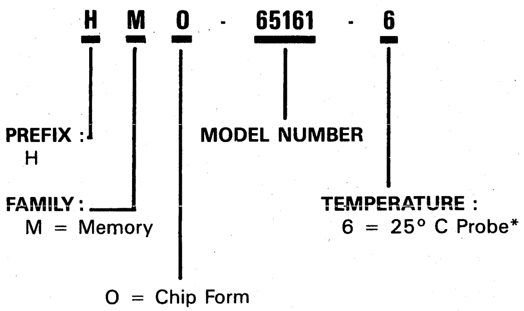
Dimensions : all chip dimensions nominal with a tolerance of ± .003''. Maximum chip thickness is .023''.

Bonding Pads : Minimum bonding pad size is .004'' × .004'' unless otherwise specified.

ELECTRICAL INFORMATION

CMOS : Die substrate must be electrically connected to VCC through conductive die attach, to assure proper electrical operating characteristics.

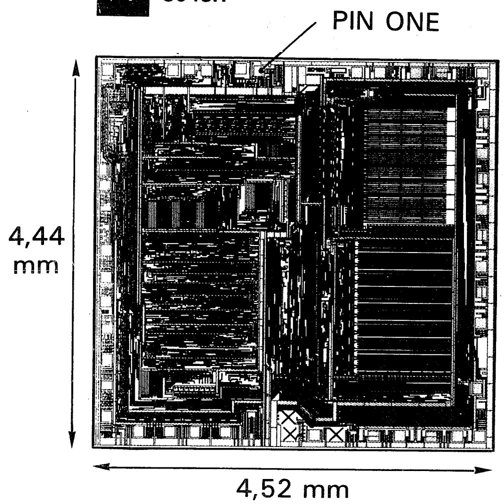
PRODUCT CODE EXAMPLE



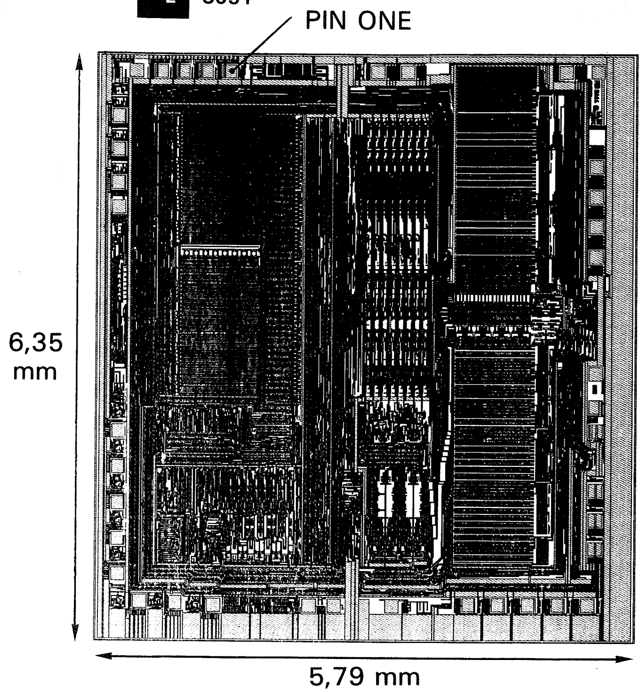
* Contact MHS for availability of – 2 (– 55° C to + 125° C) dice

11

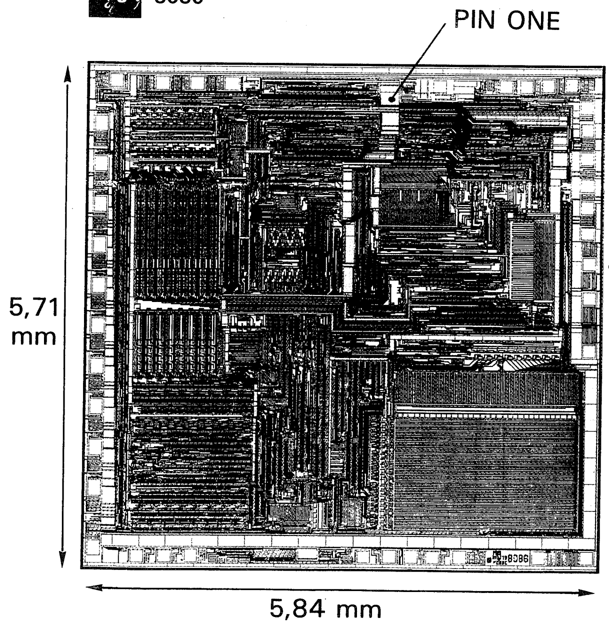
1 8048H



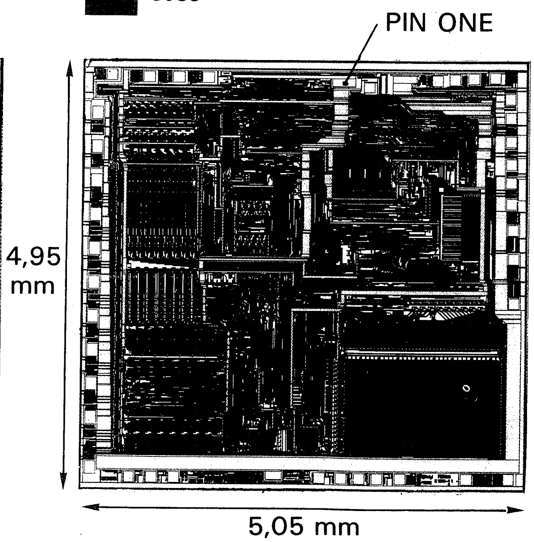
2 8051



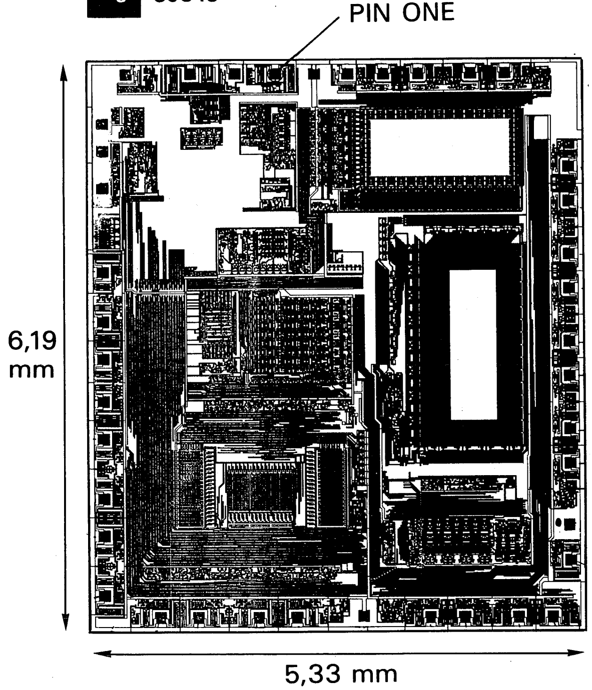
3 8086



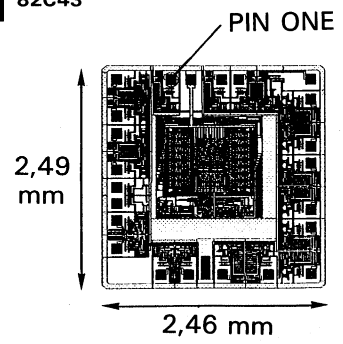
4 8088



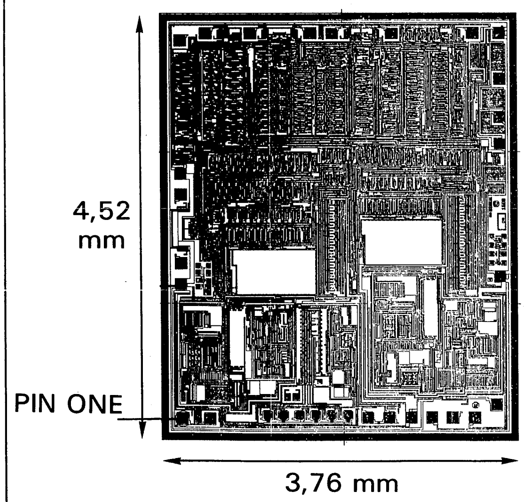
5 **80C48**



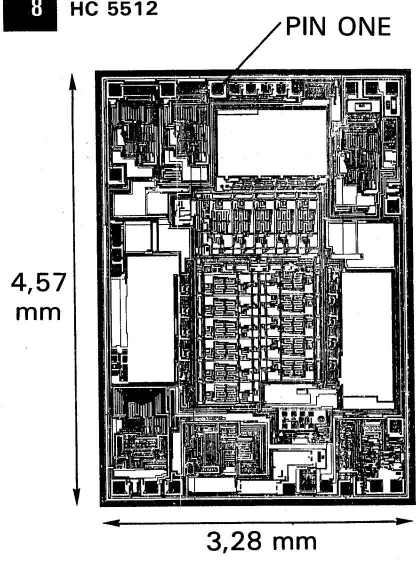
6 **82C43**



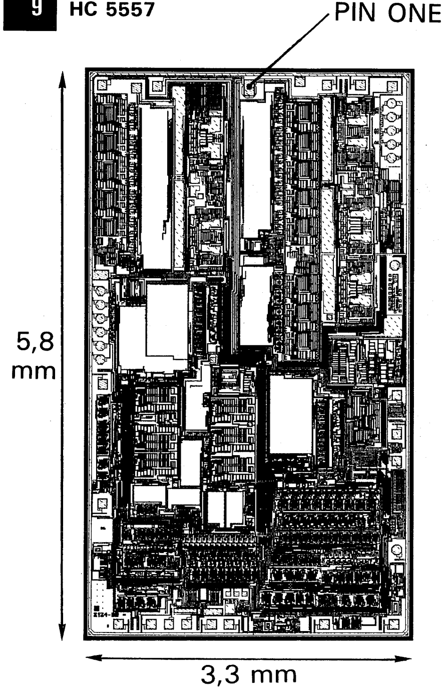
7 **HC 5510**



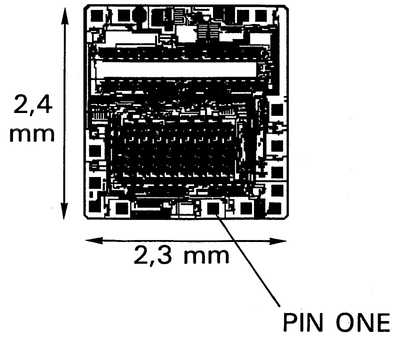
8 **HC 5512**



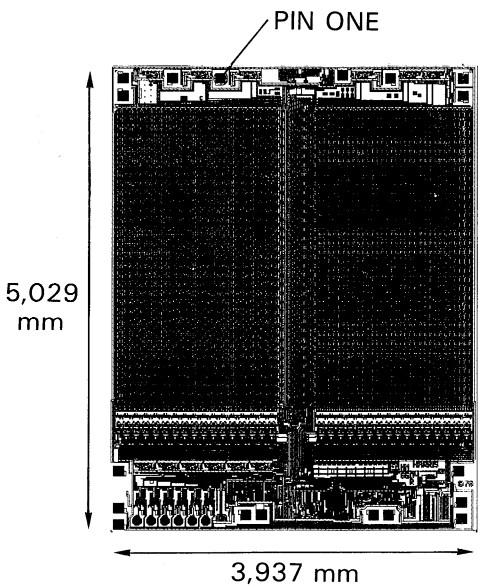
9 **HC 5557**



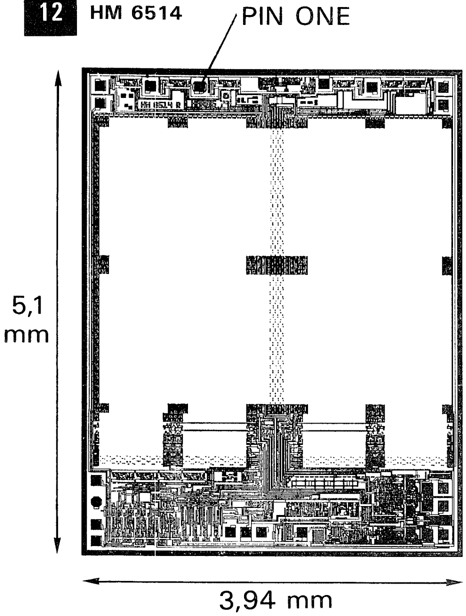
10 **HC 5589**



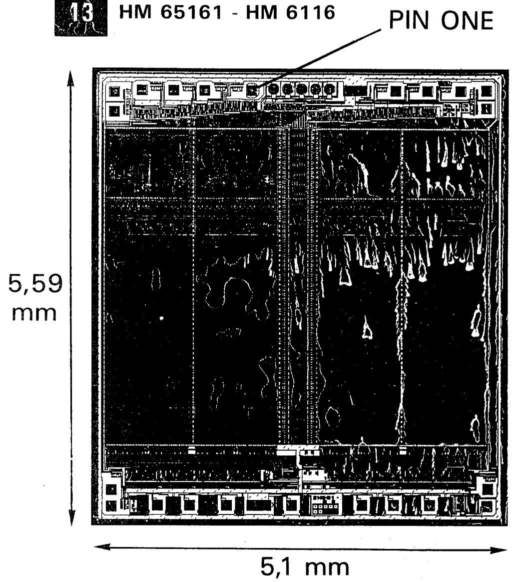
11 **HM 6504**



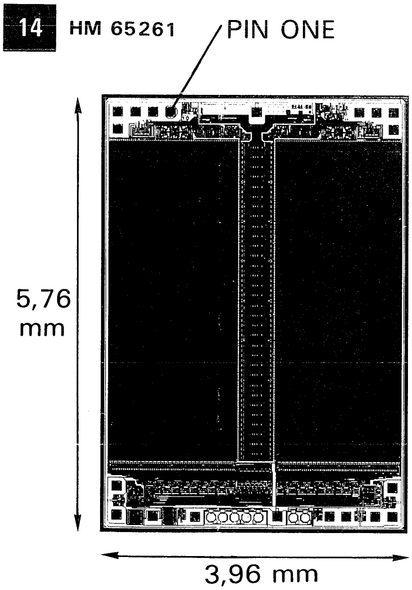
12 HM 6514



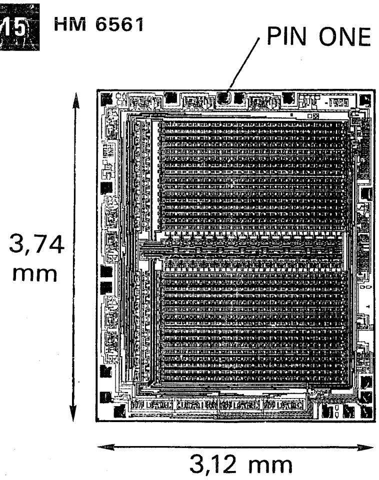
13 HM 65161 - HM 6116



14 HM 65261



15 HM 6561



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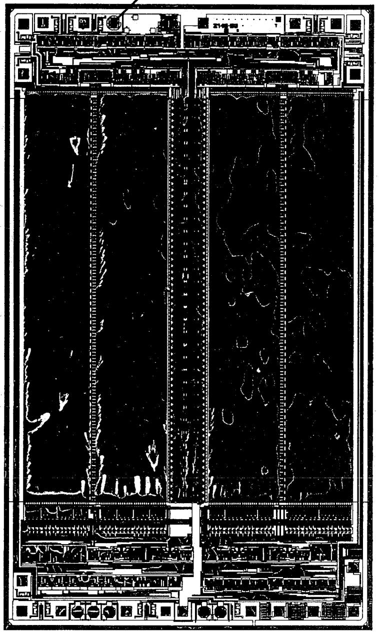
16 HM 65681

PIN ONE

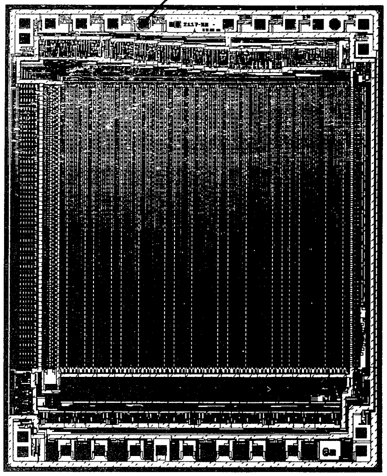


6,55 mm

3,84 mm

17 HM 6816A

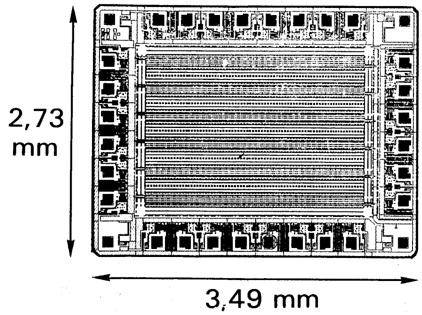
PIN ONE



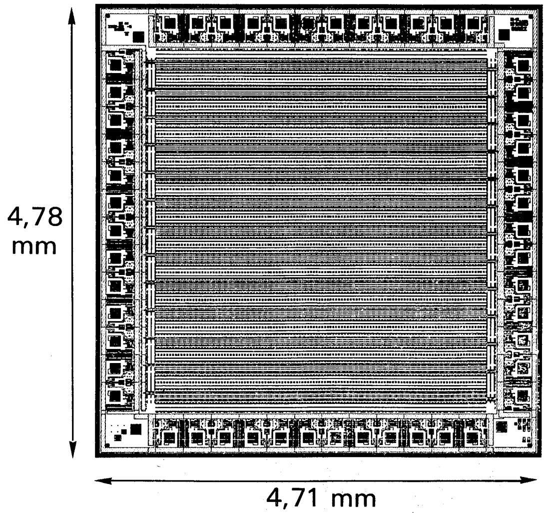
4,9 mm

3,91 mm

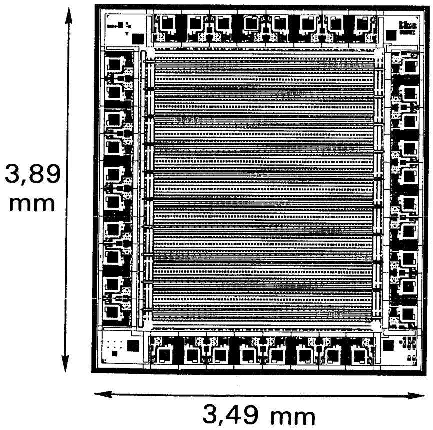
19 **MA 0250**



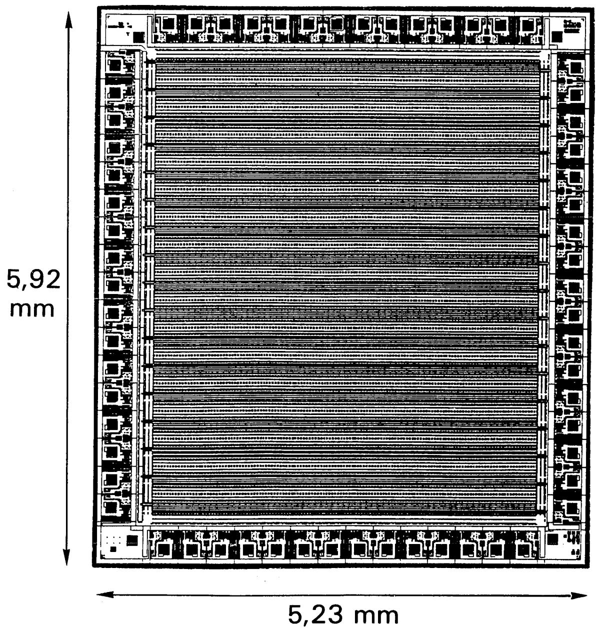
20 **MA 0800**



21 **MA 0400**



22 **MA 1200**



MHS SALES LOCATIONS

ELECTRONIC CENTER

La Chantrerie/Route de Gachet
BP 942
44075 Nantes

Phone number (international) :	(33-40) 30.30.30
national :	40-30.30.30
Twx :	711 930
Telecopy .	INFOTEC 6000

SALES OFFICE

6, avenue Charles-de-Gaulle
78150 Le Chesnay

Phone number (international) :	(33-3) 954.80.00
national :	3-954.80.00
Twx :	697 317

DISTRIBUTORS

ALMEX S.A.
Zone industrielle
48, rue de l'Aubépine
92160 Antony

Phone number (international) :	(33-1) 666.21.12
national :	1-666.21.12
Twx :	250 067

A2M
18, avenue Dutartre
78150 Le Chesnay

Phone number (international) :	(33-3) 954.91.13
national :	3-954.91.13
Twx :	698 376

EPROM
185, rue de Lyon
13015 Marseille

Phone number (international) :	(33-91) 02.97.76
national :	91-02.97.76
Twx :	400 622

FEUTRIER RHONE-ALPES
Rue des Trois-Glorieuses
42270 Saint-Priest-en-Jarez

Phone number (international) :	(33-77) 74.67.33
national :	77-74.67.33
Twx :	300 021

FEUTRIER PROVENCE
Z.I. - Avenue Laplace
13470 Carnoux

Phone number (international) :	(33-42) 82.16.41
national :	42-82.16.41

RTF
Avenue du Parc
Escalquens
31320 Castanet-Tolosan

Phone number (international) :	(33-61) 81.53.65
national :	61-81.53.65
Twx :	520 927

SPETELEC
Tour Europa III
94532 Rungis Cedex

Phone number (international) :	(33-1) 686.56.65
national :	1-686.56.65
Twx :	250 801

Harris-MHS sales locations

EUROPEAN SALES HEADQUARTER

HARRIS-MHS
Einsteinstrasse 127
8000 Munich 80
West Germany
Phone number (international) : (49-89) 47.30.47
national : 089-47.30.37
Twx : 524 126

SALES OFFICES

HARRIS-MHS
P.O. Box 27
153, Farnham road
Slough SL 1 4XD
England
Phone number (international) : (44-753) 34.666
national : 0753-34.666
Twx : 848 174

HARRIS-MHS
Via Fratelli Gracchi 48
20092 Cinisello Balsamo
Milano Italy
Phone number (international) : (39-2) 618.82.82
national : 02-618.82.82
Twx : 311 164

HARRIS-MHS
Erfurterstrasse 29
8057 Eching
West Germany
Phone number (international) : (49-89) 319.10.35
national : 089-319.10.35
Twx : 521 3866

HARRIS-MHS
Walsroderstrasse 71
3012 Langenhagen
West Germany
Phone number (international) : (49-511) 73.70.37
national : 0511-73.70.37
Twx : 923 04 74

EUROPEAN DISTRIBUTORS

AUSTRIA

TRANSISTOR VERTRIEBSGES. MbH & Co. KG
Auhofstrasse 41 A
1130 Wien
Phone number (international) : (43-222) 82.94.01
national : 0222-82.94.01
Twx : 13 37 38

BELGIUM

BETEA S.A.
775, Chaussée de Louvain
1140 Brussels
Phone number (international) : (32-2) 736.80.50
national : 02-736.80.50
Twx : 231 88

DENMARK

DITZ SCHWEITZER A.S.
Vallensbaekvej 41
2600 Glostrup
Phone number (international) : (45-2) 45.30.44
national : 02-45.30.44
Twx : 33 257

FINLAND

YLEISELEKTRONIIKKA OY
Atomitie 5b
PL 33
00370 Helsinki 37
Phone number (international) : (358-90) 562.11.22
national : 090-562.11.22
Twx : 123 212

GERMANY

ALFRED NEYE ENATECHNIK GmbH
Schillerstrasse 14
2085 Quickborn

Phone number (international) :	(49-4106) 6120
national :	04106-6120
Twx :	2 135 90

JERMYN GmbH
Schulstrasse 84
6277 BAD Camberg

Phone number (international) :	(49-6434) 230
national :	06434-230
Twx :	4 844 26

KONTRON Halbleiter GmbH
Breslauerstrasse 2
8037 Eching

Phone number (international) :	(49-89) 31.90.10
national :	089-31.90.10
Twx :	5 221 22
Telefax	089.31901.311

SASCO GmbH
Hermann-Oberth-Strasse 16
8011 Putzbrunn

Phone number (international) :	(49-89) 46.11.1
national :	089-46.11.1
Twx :	5 295 04

SPOERLE ELECTRONIC
Handelsgesellschaft MBH + Co.
Max-Planck-Strasse 1-3
Postfach 10.21.40
D-6072 Dreieich

Phone number (international) :	(49-6103) 304.1
national :	06103-304.1
Twx :	4 179 03/4 179 83

ISRAEL

M.R.B.D. Ltd.
54 Jabotinsky Street
P.O.B. 1717
Ramat-Gan 52-117

Phone number (international)	(972-3) 732.624
national :	03.732.624
Twx :	341467

ITALY

LASI ELETTRONICA S.P.A.
Viale Lombardia 6
20092 Cinisello Balsamo (Milano)

Phone number (international) :	(39-2) 612.04.41
national :	02-612.04.41
Twx :	331 612

ELEDRA
3S SPA
V. Le Elvezia 18
20154 Milano

Phone number (international) :	(39-2) 34.97.51
national :	02-34.97.51
Twx :	331 612

NETHERLANDS

TECHMATION ELECTRONICS B.V.
Bernhardstraat 11
4175 ED Haaften
P.O.B. 9
4175 ZG Haaften

Phone number (international) :	(31-4189) 2222
national :	04189-2222
Twx :	50423

NORWAY

NATIONAL ELEKTRO A/S
Ulvenveien 75
P.O. Box 75
Oekern
Oslo 5
Phone number (international) : (47-2) 64.49.70
national : 02-64.49.70
Twx : 712 65

SPAIN & PORTUGAL

UNITRONICS S.A.
Plaza Espana 18
Madrid 13
Phone number (international) : (34-2) 242.52.04
national : 02-242.52.04 & 448.01.62
Twx : 46 786 & 22 596

SWEDEN

AB BETOMA
P.O. Box 3005
171 03 Solna
Phone number (international) : (46-8) 82.02.80
national : 08-82.02.80
Twx : 19 389

SWITZERLAND

STOLZ AG
Täfernstrasse 15
5054 Baden-Dättwill
Phone number (international) : (41-56) 84.01.51
national : 056-84.01.51
Twx : 54 070

UNITED KINGDOM

HY-COMP. Ltd.
11 Shield road
Ashford industrial estate
Ashford TW 15 1 AV
Middlesex
Phone number (international) : (44-7842) 46273
national : 07842-46273
Twx : 923 802

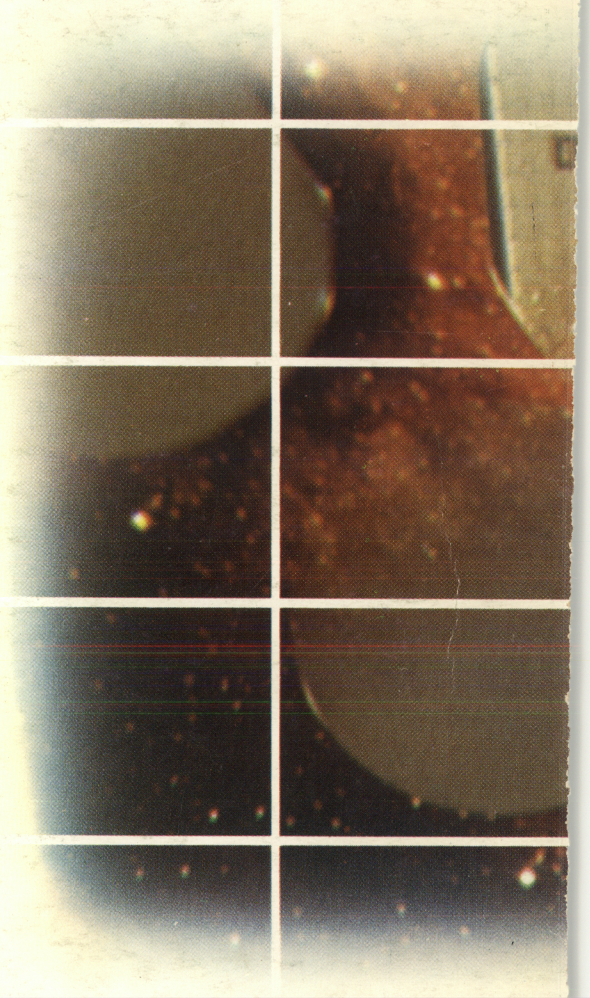
MACRO MARKETING Ldt.
Burhnam Lane
Slough SL 1 6 LN
Berkshire
Phone number (international) : (44-6286) 4422
national : 06286-4422
Twx : 847 945

RADIO RESISTOR CO Lt.
St Martins Way
Industrial Estate
Cambridge Road
Bedford
MK-42 OLF
Phone number (international) : (44-0234) 47211
national : 0234-47211
Twx : 826 251

THAME COMPONENTS Ltd.
Thame Park Road
Thame
Oxon OX9 3XD
Phone number (international) : (44-84421) 4561
national : 084421-4561
Twx : 837 917

SCOTLAND REPRESENTATIVE

PHOENIX ELECTRONICS (AIRDRIE) Ltd.
Western Buildings
Vere road
Kirkmuirhill
ML 11 9RP Lanarkshire
Scotland
Phone number (international) : (44-555) 892.393
national : 0555-892.393
Twx : 777 404



MHS
MATRA-HARRIS SEMICONDUCTEURS

EDITION 83-11-DI-C-76

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